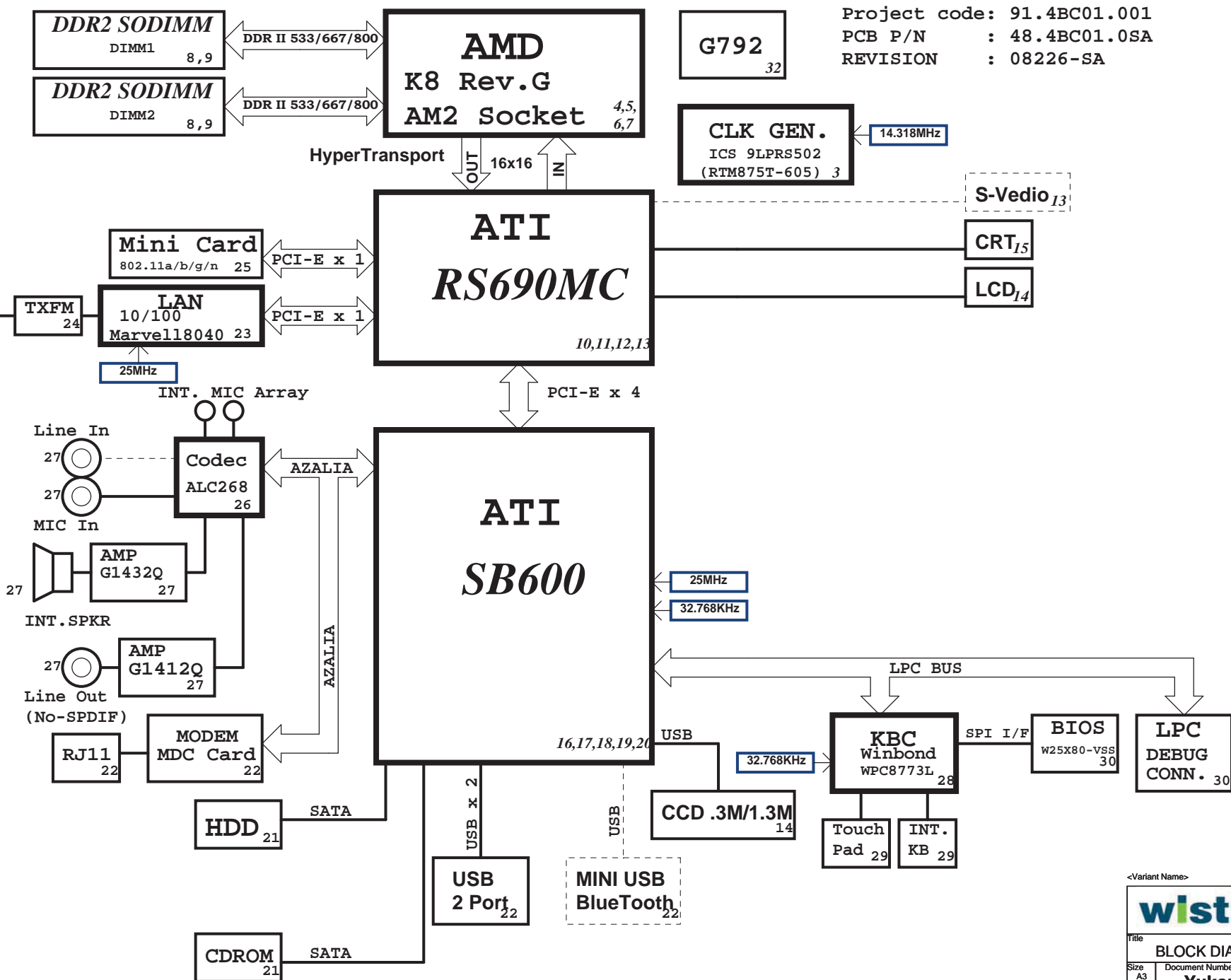


# Yukon Block Diagram



### PCB Layer Stackup

**L1: Signal 1**  
**L2: VCC**  
**L3: Inner Signal 2**  
**L4: Inner Signal 3**  
**L5: GND**  
**L6: Signal 4**

## CPU V\_CORE

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>VCC_CORE_S0</i>

## SYSTEM DC/DC

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>ID2V_S0</i> <i>ID8V_S3</i>

## SYSTEM DC/DC

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>5V_S5</i> <i>3D3V_S5</i>

## SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

---

**SYSTEM LDO**

INPUT	OUTPUT
3D3V_S5	1D2V_S5
3D3V_S0	2D5V_S0
3D3V_S0	1D5V_S0

## SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

### Battery Charger

INPUTS	OUTPUTS
$AD+$ $BAT+$	$DCBATOUT$

&lt;Variant Name&gt;



**Wistron Incorporated**  
21F, 88, Hsin Tai Wu Rd  
Hsichih, Taipei

Title	BLOCK DIAGRAM
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Size	Document Number
------	-----------------

Size  
A3

Document Number  
**Yukon**

Date: Thursday, July 03, 2008

Sheet 1 of 43

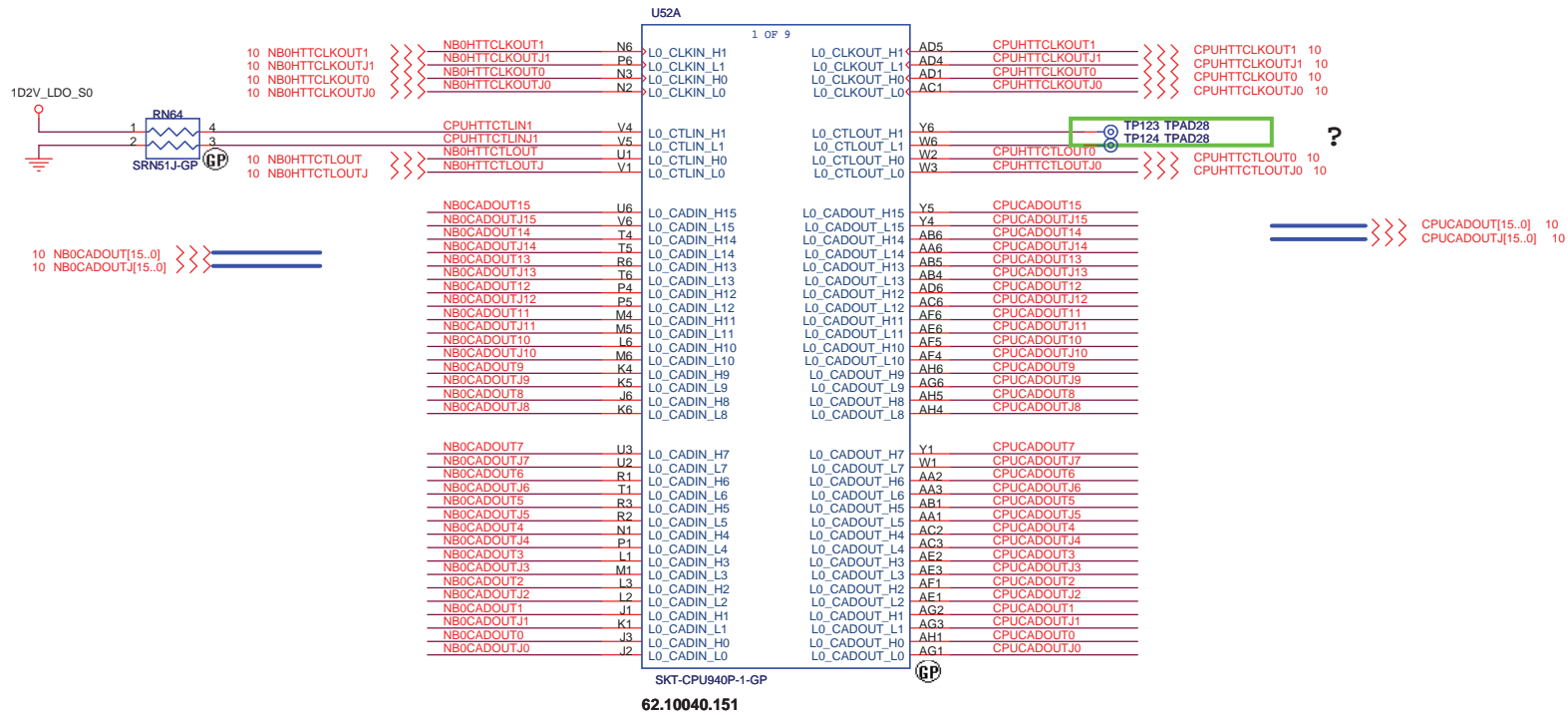
Rev
SA

	5	4	3	2	1
D					
C					
B					
A					

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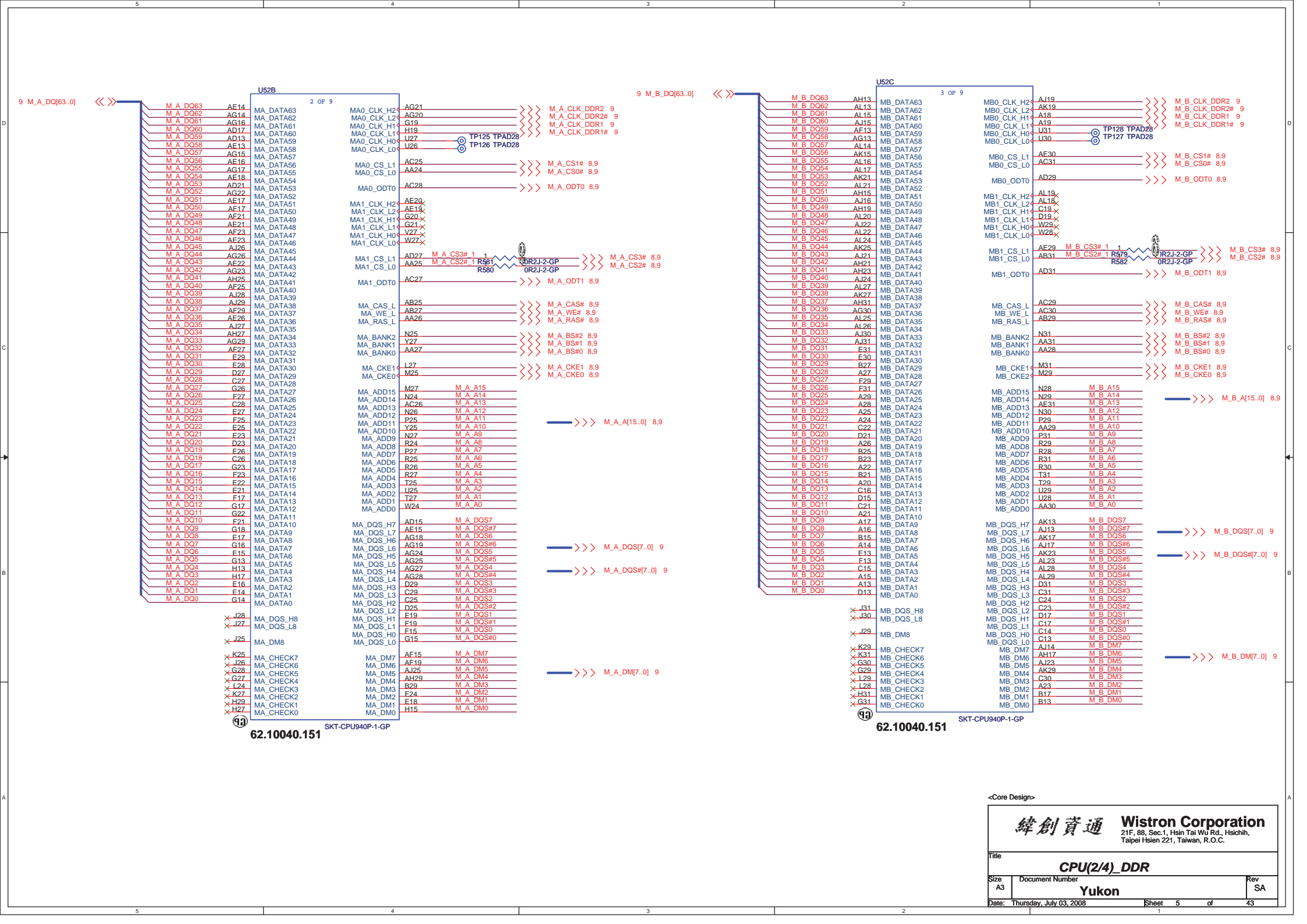
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CHANGE HISTORY			
Size	Document Number		Rev
A3	Yukon		SA
Date:	Thursday, July 03, 2008	Sheet 2 of	43

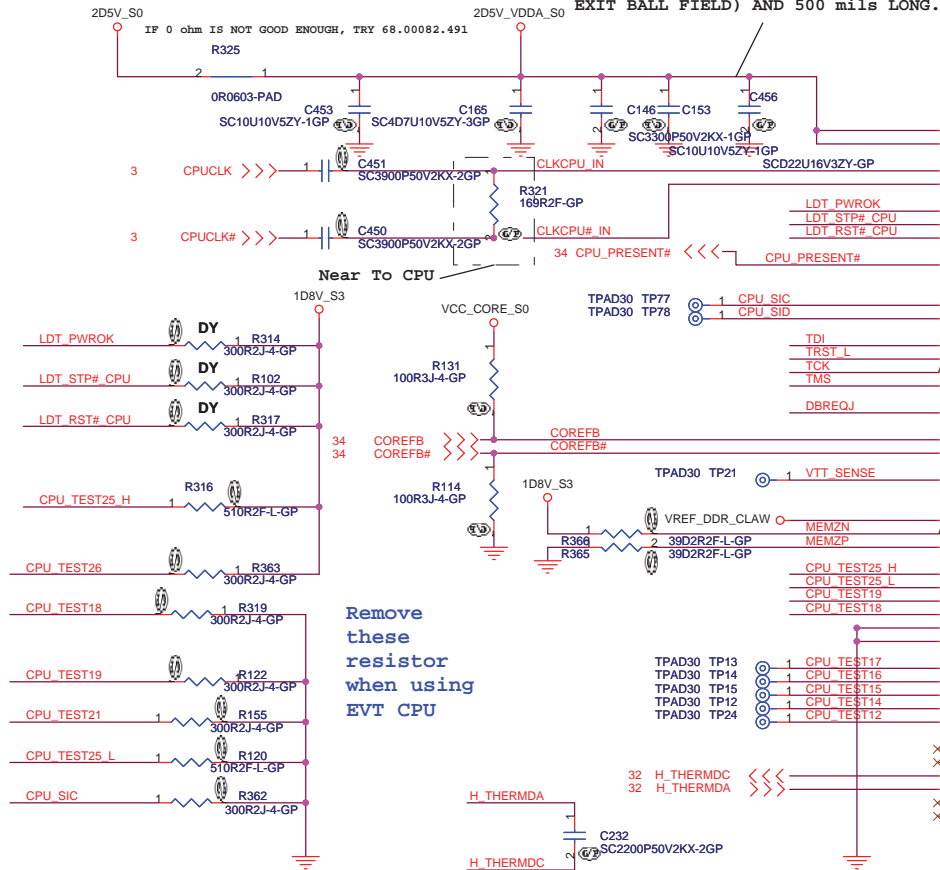


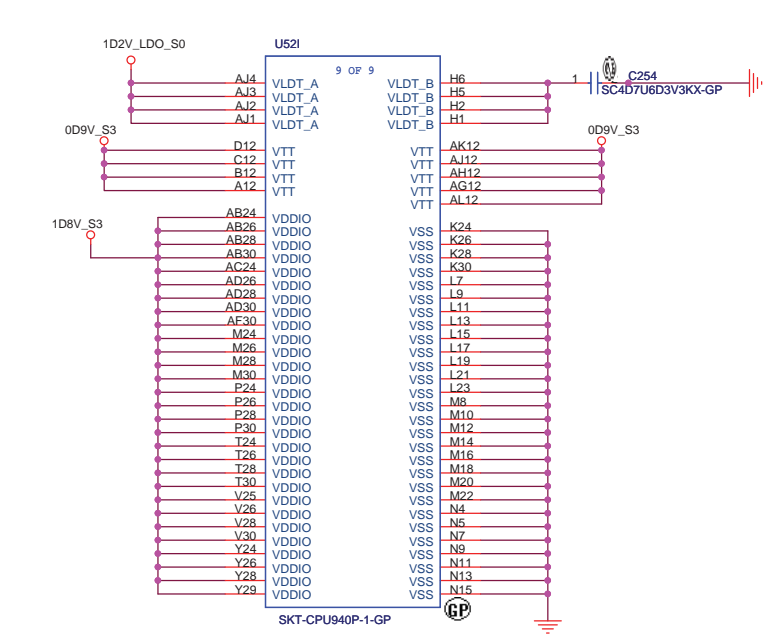


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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CPU(1/4)_HyperTransport I/F			
Size	Document Number	Rev	
A3	Yukon	SA	
Date:	Thursday, July 03, 2008	Sheet	4 of 43

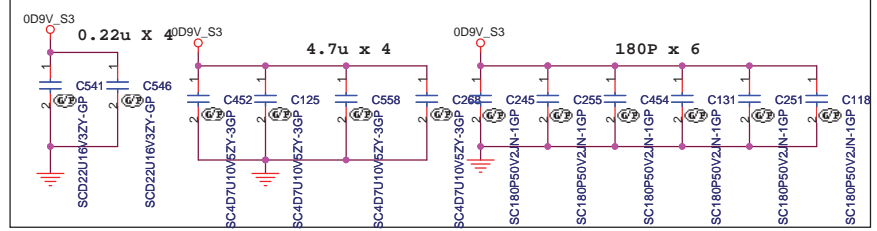




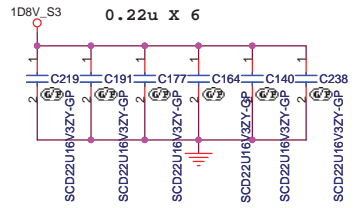
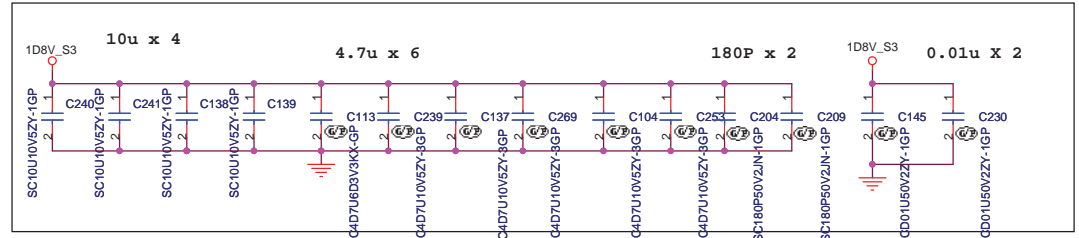
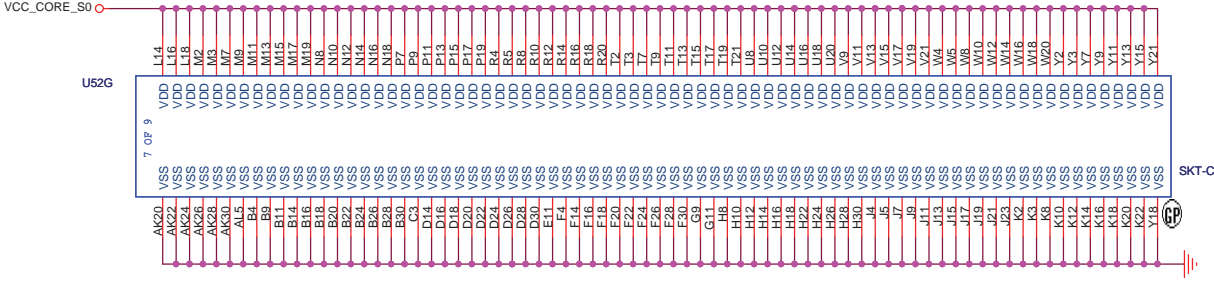
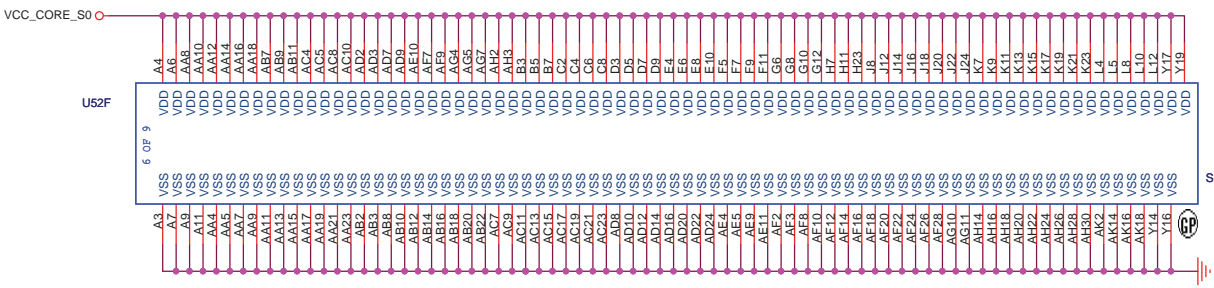
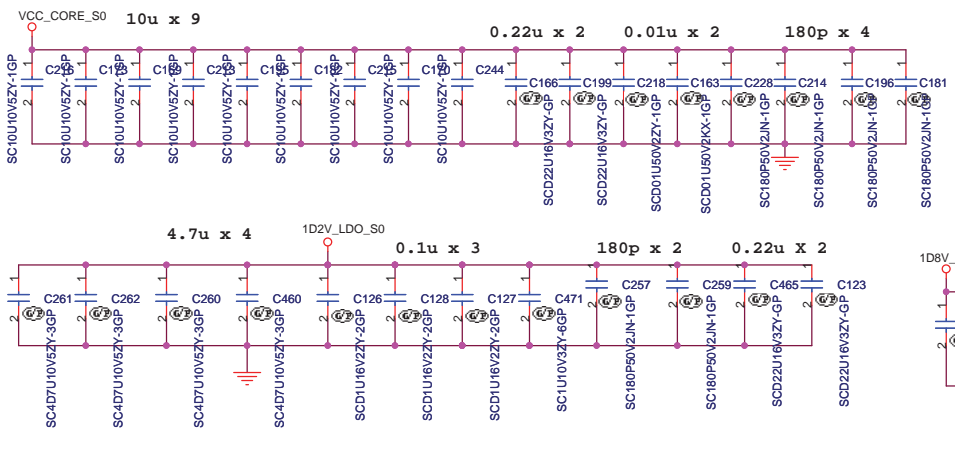


62.10040.151

Place near to CPU



LAYOUT: Place on backside of processor.



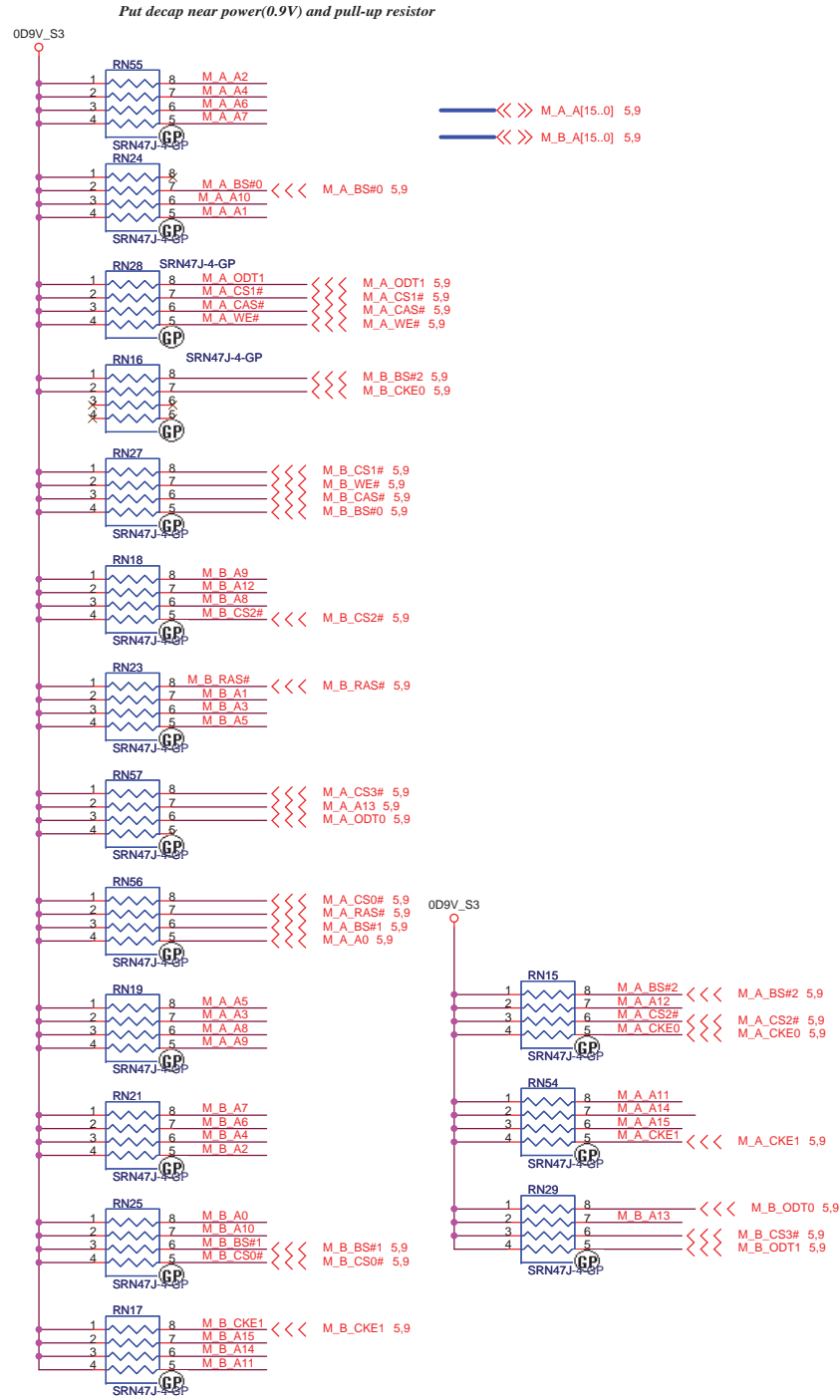
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**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

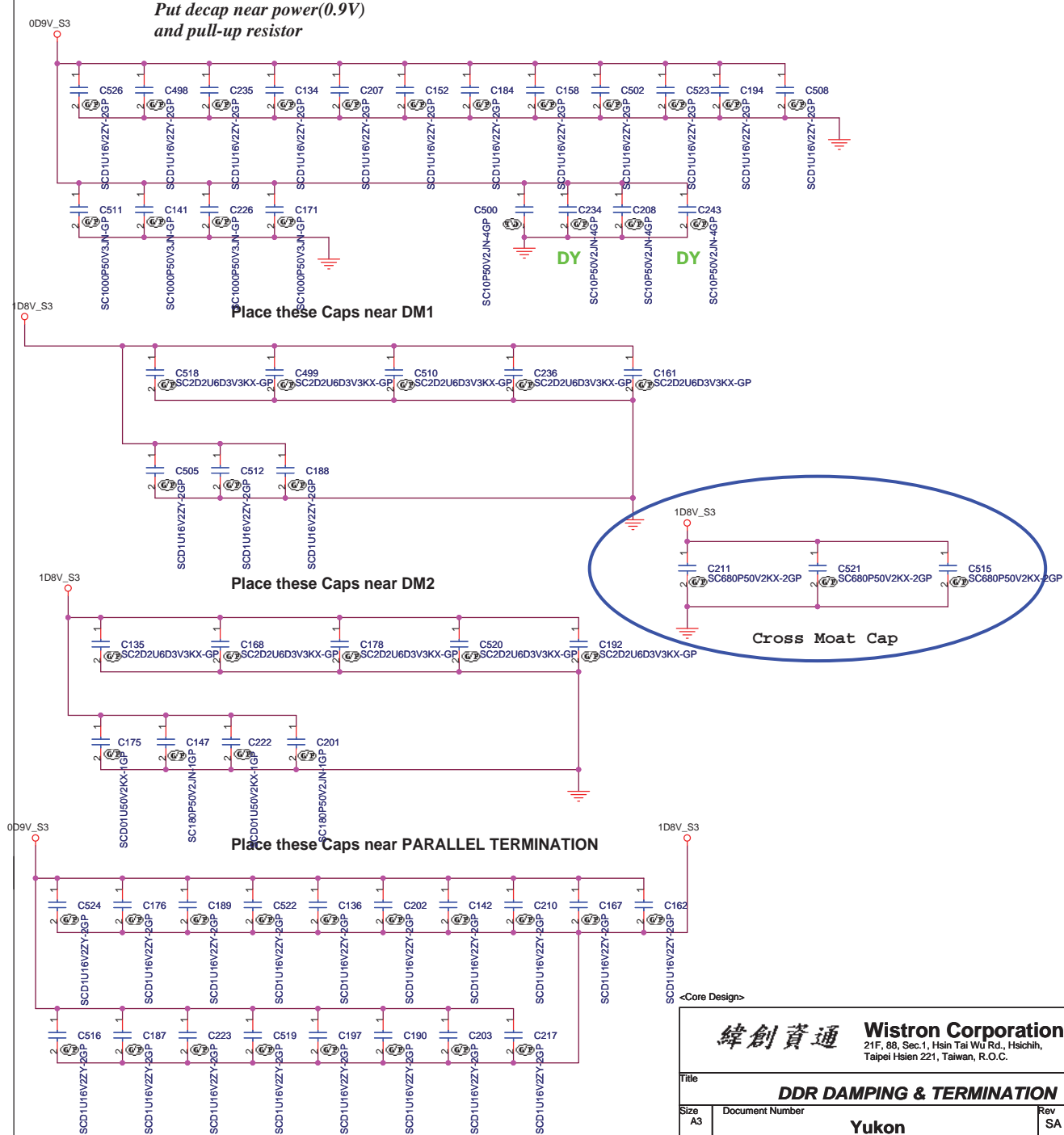
Title <b>CPU(4/4)_Power</b>		
Size A3	Document Number <b>Yukon</b>	Rev SA
Date: Tuesday, July 01, 2008		Sheet 7 of 43



PARALLEL TERMINATION

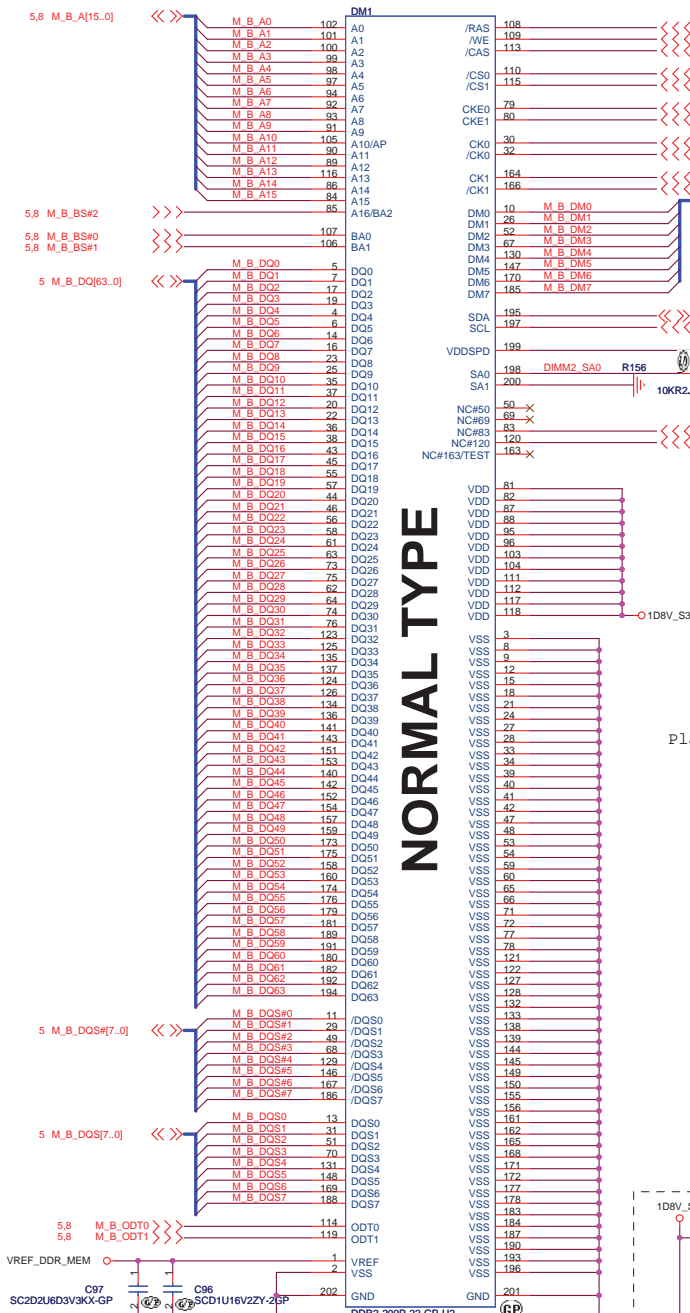


Decoupling Capacitor



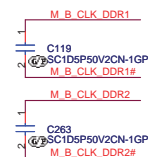


# NORMAL TYPE

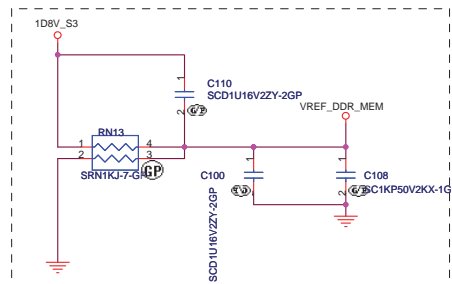


62.10017.A61  
High 9.2mm  
2nd: 62.10017.A51

Place near CPU

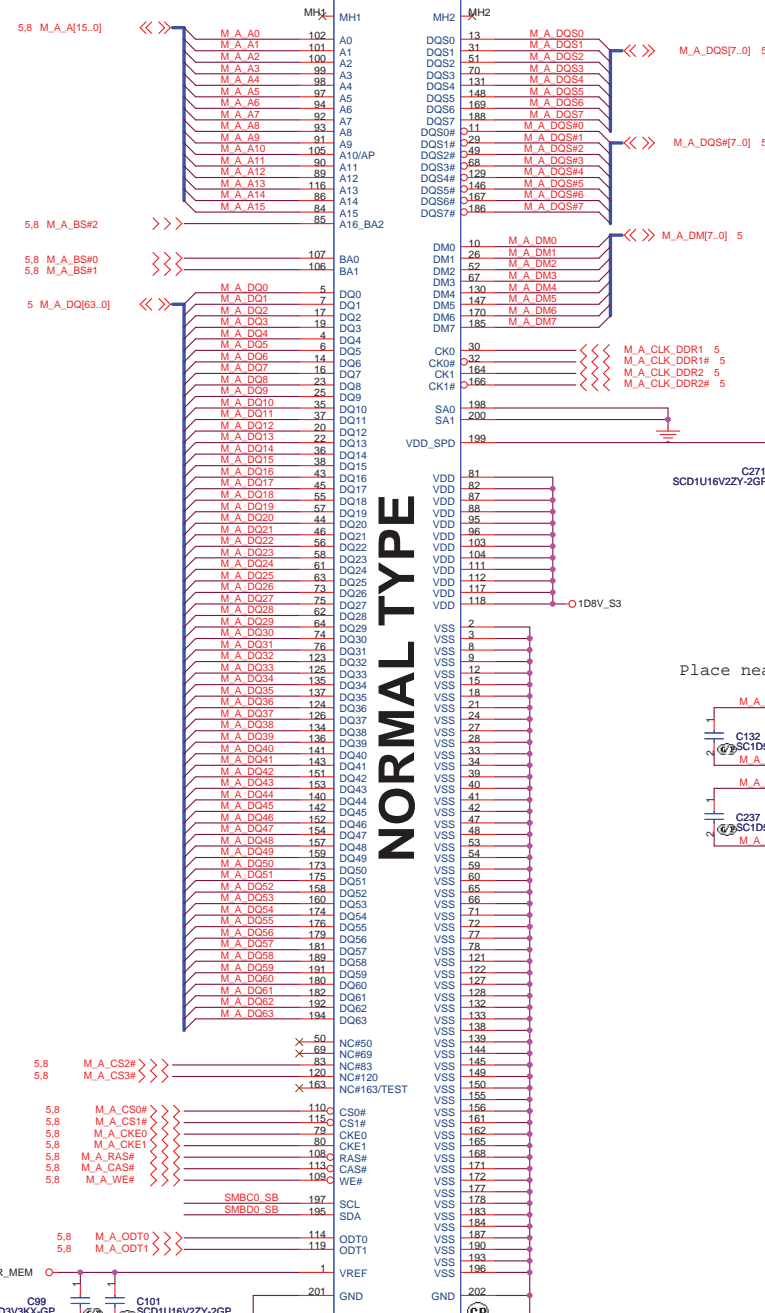


## DDR\_VREF



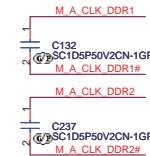
LAYOUT: Locate close to DIMM

# NORMAL TYPE



62.10017.661  
High 5.2mm  
2nd: 62.10017.A41

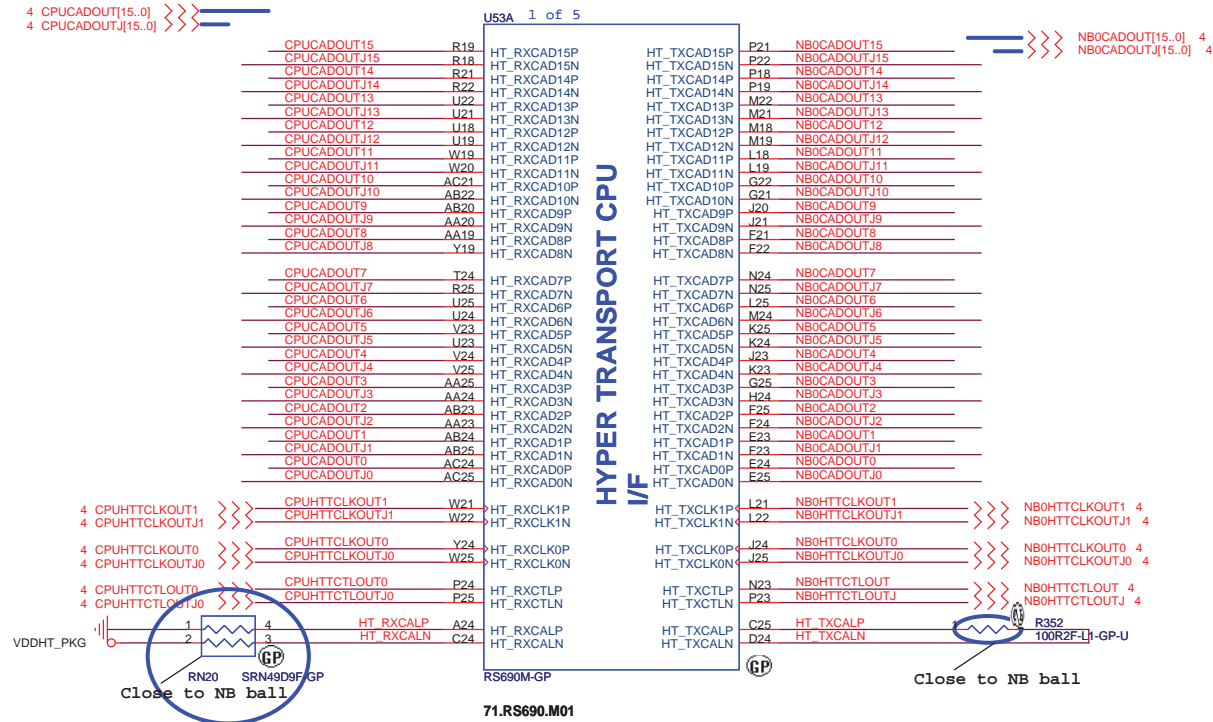
Place near CPU



Core Design			
緯創資通 Wistron Corporation			
21F, 8B, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.			
DDR SO-DIMM SKT			
File	Document Number	Rev	SA
Size	Custom	Yukon	
Date: Thursday, July 03, 2008	Sheet 9	of	43

## CLAW HAMMER TO NB

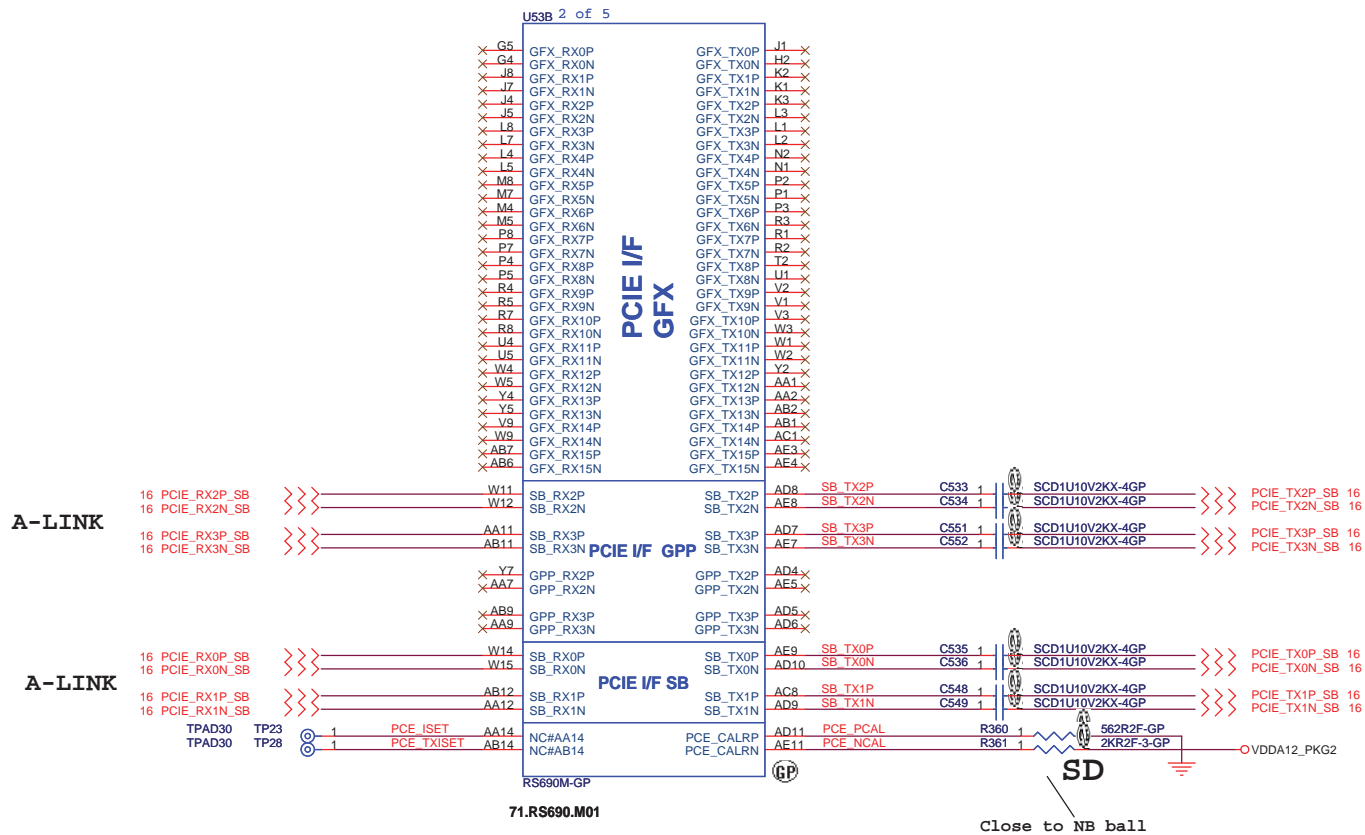
## NB TO CLAW HAMMER



&lt;Core Design&gt;

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			NB-RS690M HT	
Size	Document Number	Yukon		Rev
A3				SA
Date:	Thursday, July 03, 2008	Sheet	10 of 43	

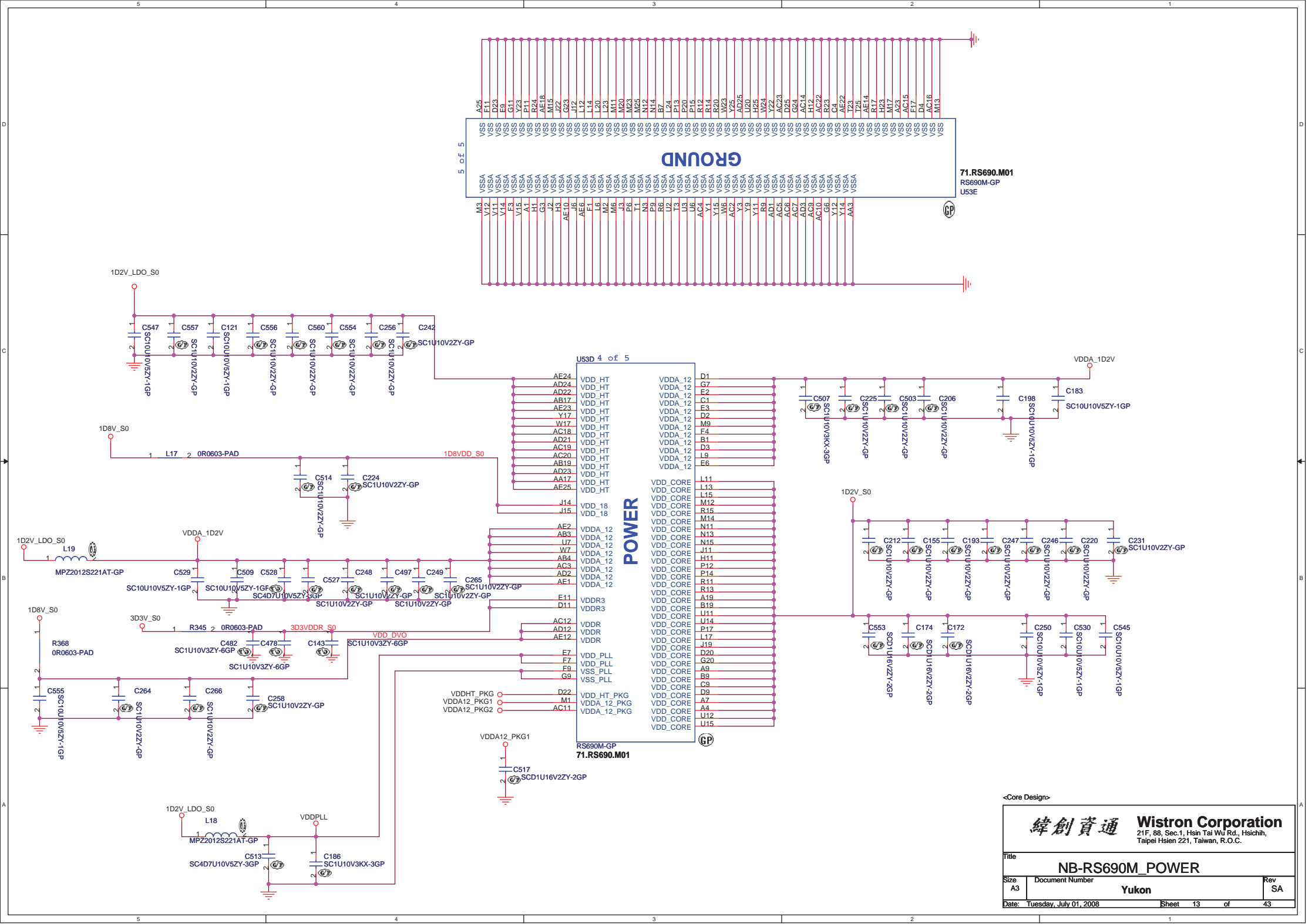


**A-LINK**  
**CLOSE TO NB**

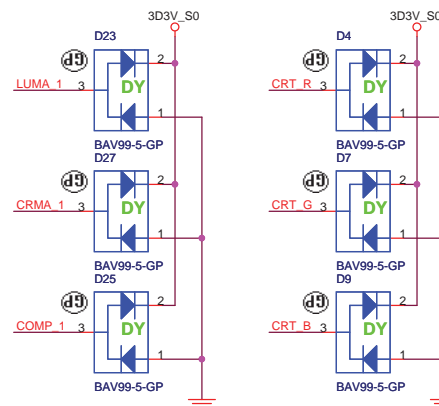
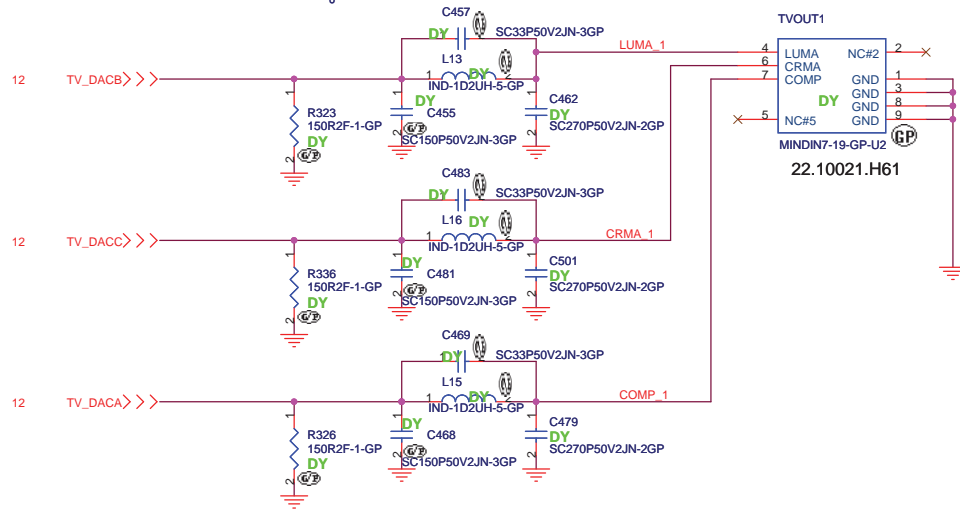
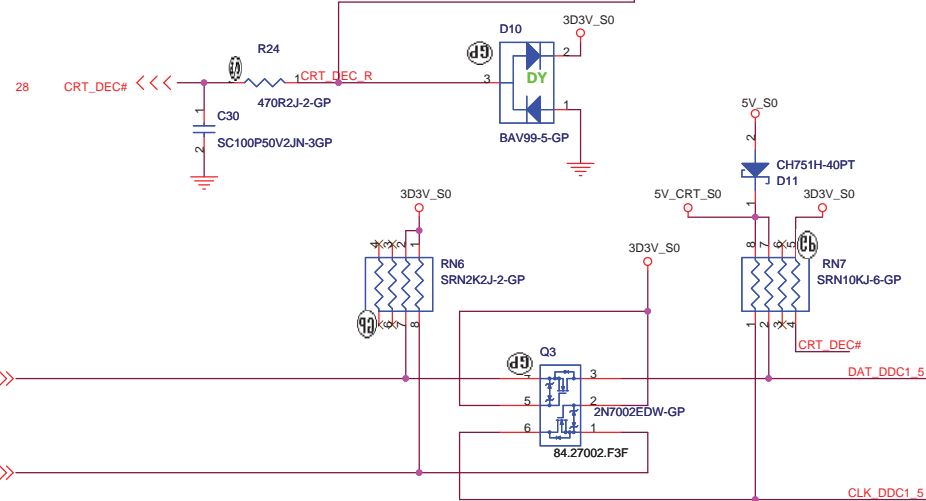
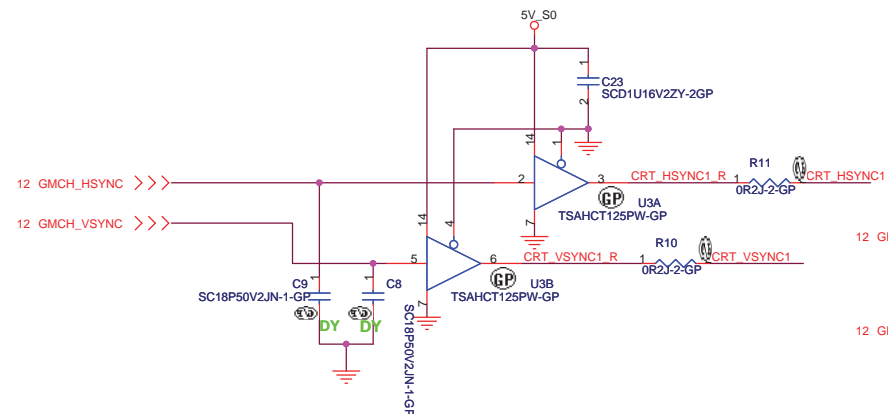
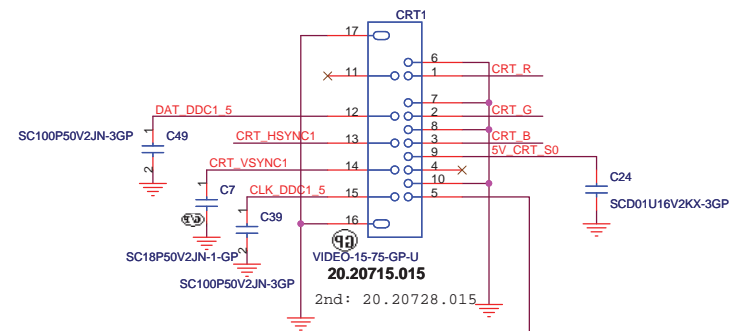
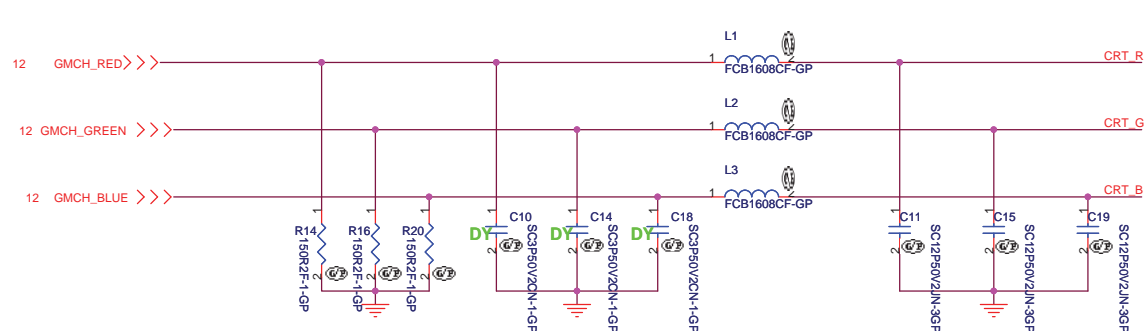
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<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
NB-RS690M_MEM/PCIE_LINK I/F			
Size	Document Number		Rev
A3	<b>Yukon</b>		SA
Date:	Thursday, July 03, 2008	Sheet 11 of 43	






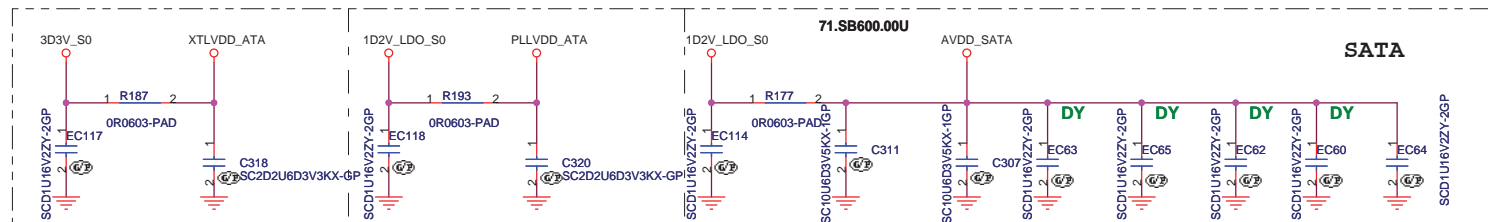
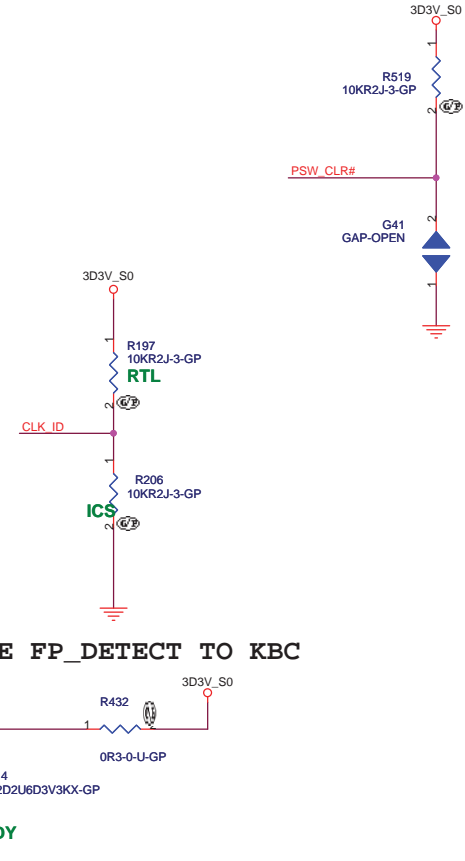
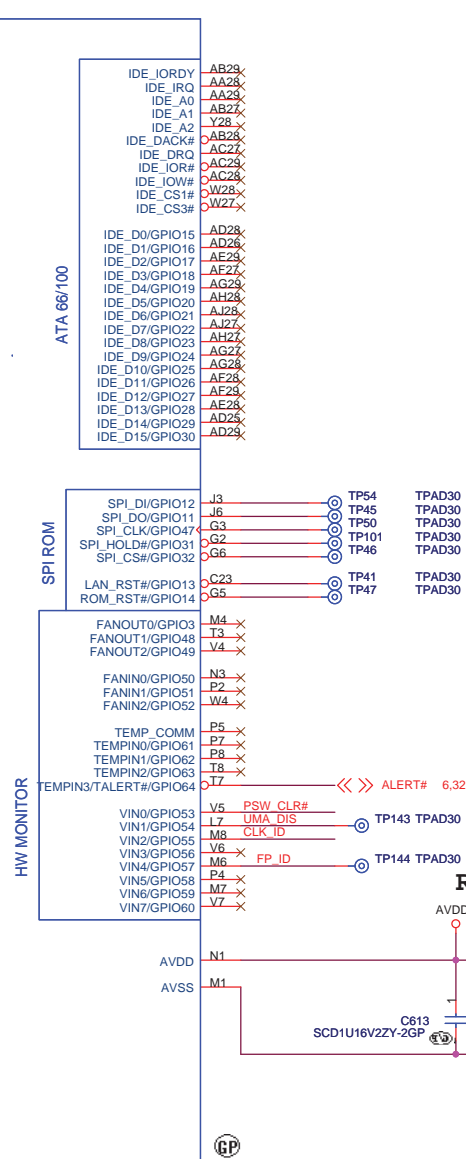
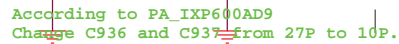
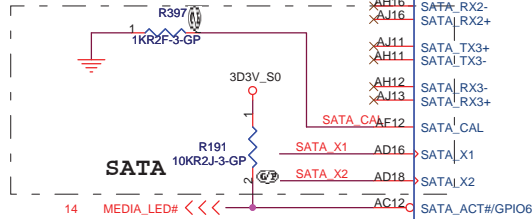


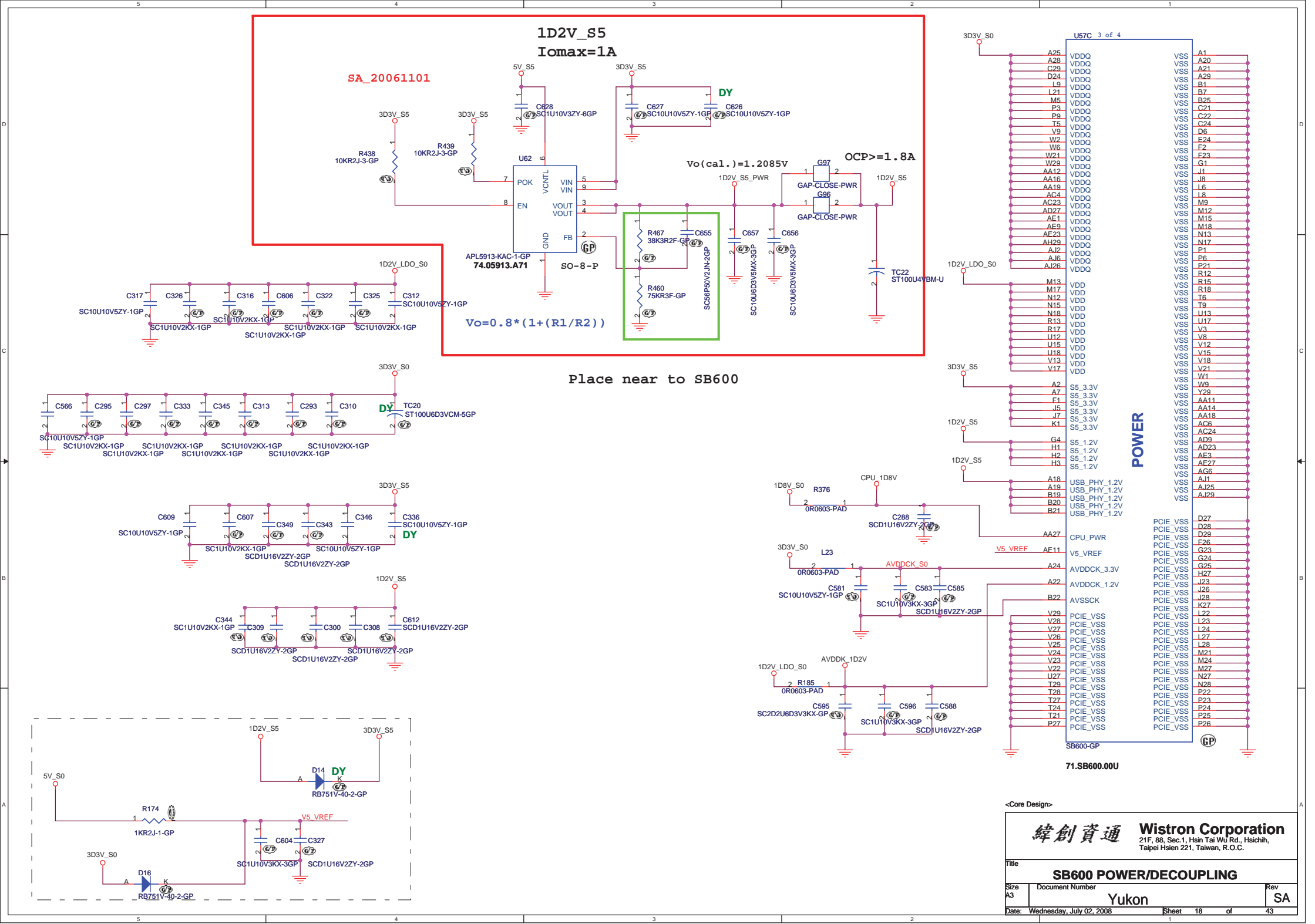


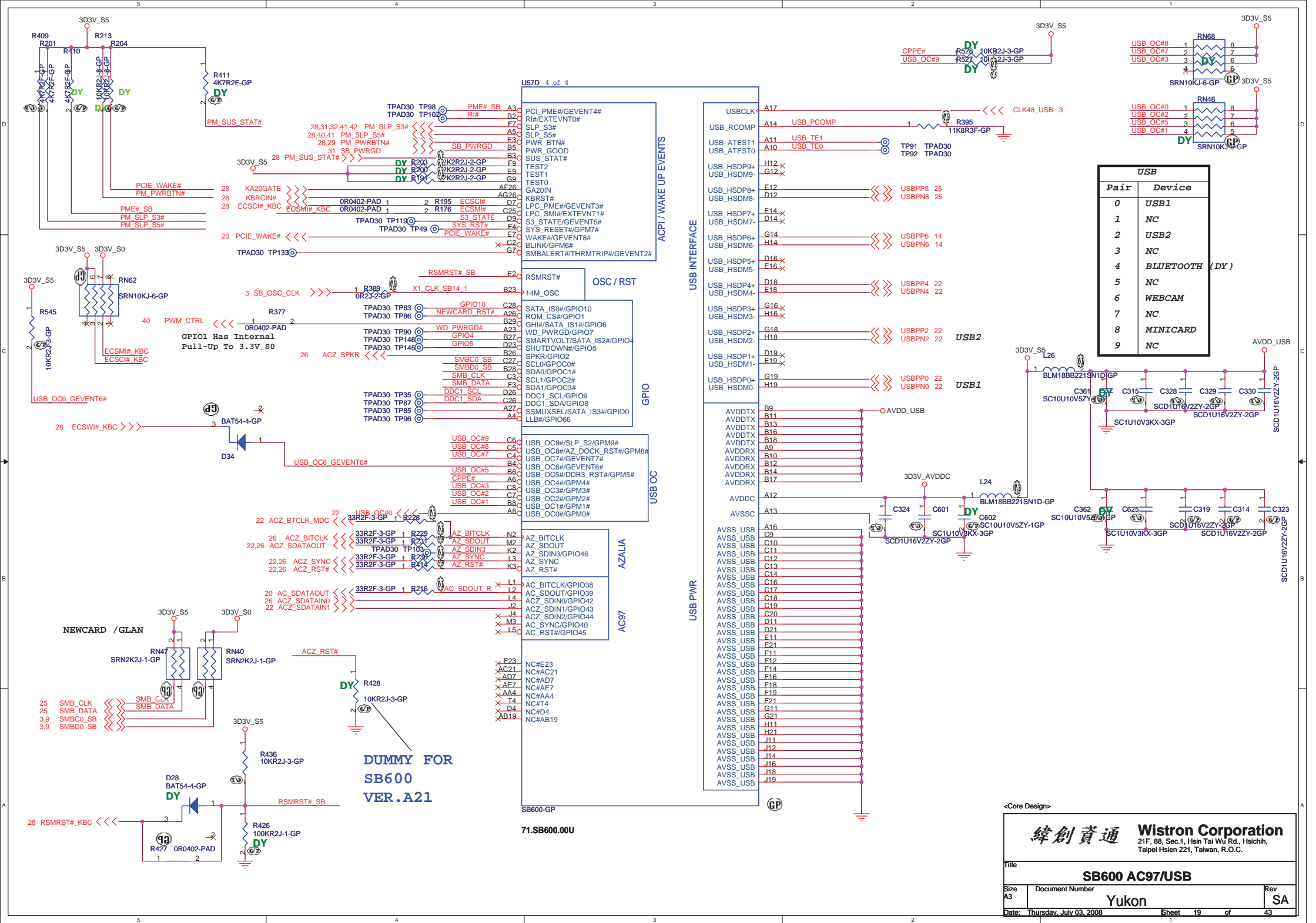


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Title				
SB600 PCI/CPU/LPC/RTC (1 of 5)				
Size A3	Document Number	Yukon		Rev SA
Date:	Thursday, July 03, 2008	Sheet	16 of	43

										U57B 2 of 4	
21	SATA_TXP0	<<<	C586	1	SCD01U50V2KX-1GP	SATA_TXP0_SB	AH21	SATA_TX0+			
21	SATA_TXN0	>>>	C587	1	SCD01U50V2KX-1GP	SATA_TXN0_SB	AJ21	SATA_TX0-			
21	SATA_RXN0	>>>	C590	1	SCD01U50V2KX-1GP	SATA_RXN0_SB	AH20	SATA_RX0-			
21	SATA_RXP0	<<<	C593	1	SCD01U50V2KX-1GP	SATA_RXP0_SB	AJ20	SATA_RX0+			
21	SATA_TXP1	<<<	C710	1	SCD01U50V2KX-1GP	SATA_TXP1_SB	AH18	SATA_TX1+			
21	SATA_TXN1	>>>	C712	1	SCD01U50V2KX-1GP	SATA_TXN1_SB	AJ18	SATA_TX1-			
21	SATA_RXN1	>>>	C713	1	SCD01U50V2KX-1GP	SATA_RXN1_SB	AH17	SATA_RX1-			
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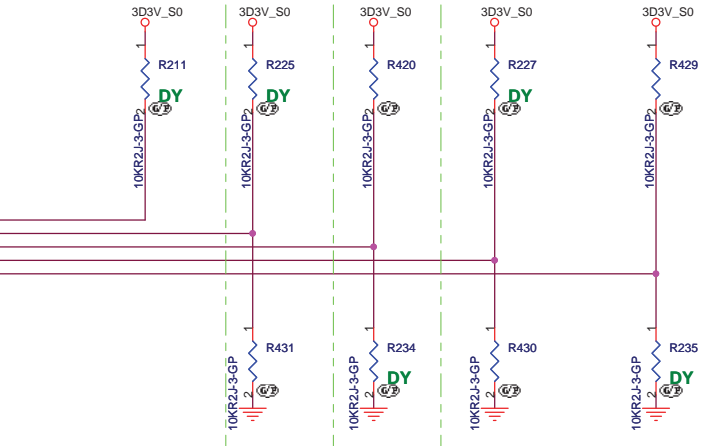






PCI\_CLK4  
PCI\_CLK6  
PCI\_CLK0  
PCI\_CLK1

19 AC\_SDATAOUT  
16,28 PCLK\_KBC  
15 CLK33\_LPCROM  
16,28 PCI\_CLK0  
16 PCLK\_PCM

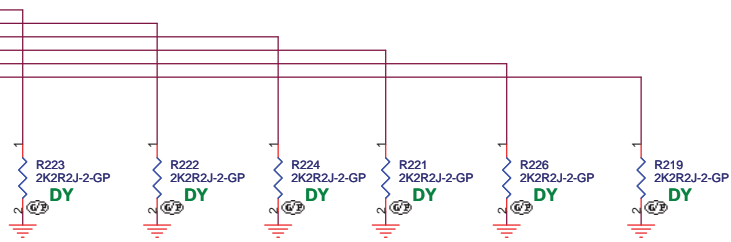


REQUIRED SYSTEM STRAPS

		SB600				
		AC_SDOOUT	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM		
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4	DEFAULT		

SB600 HAS 15K INTERNAL PU FOR PCI\_AD[23..28]

16 PCI\_AD28  
16 PCI\_AD27  
16 PCI\_AD26  
16 PCI\_AD25  
16 PCI\_AD24  
16 PCI\_AD23



DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

SB600 STRAPPING PIN

Size A3

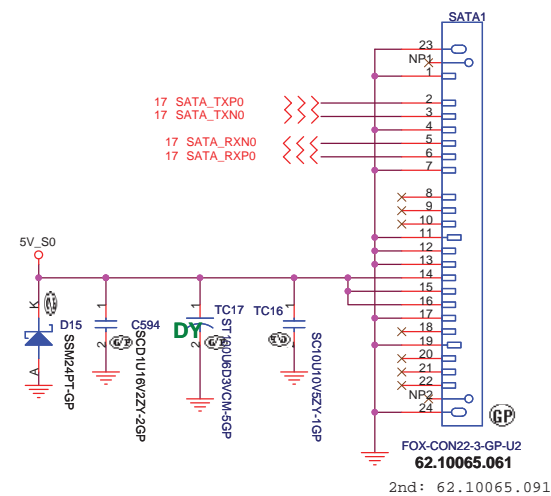
Document Number

Rev SA

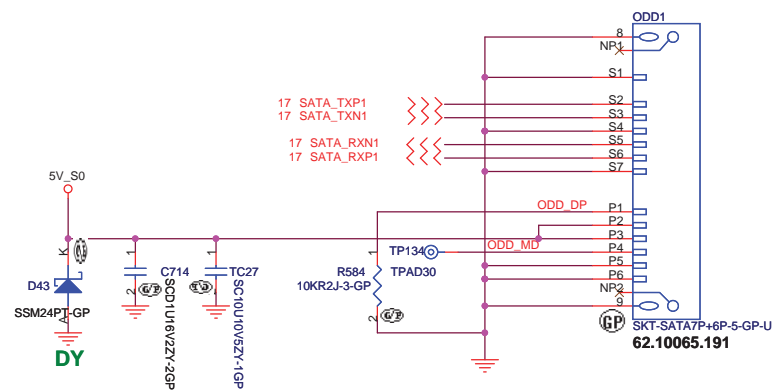
Date: Thursday, July 03, 2008

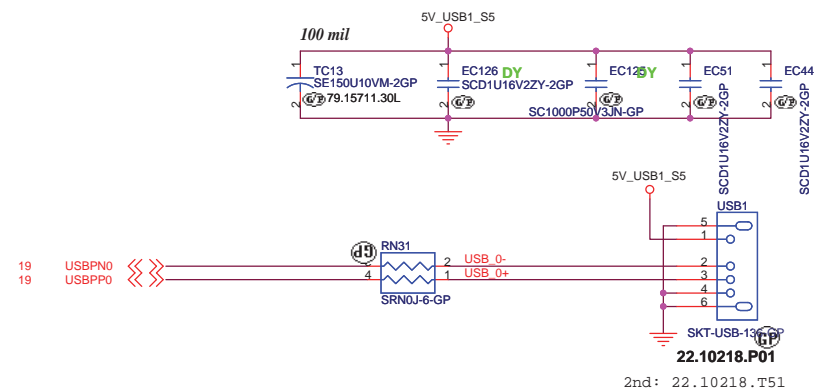
Sheet 20 of 43

SATA HD Connector



SATA ODD Connector



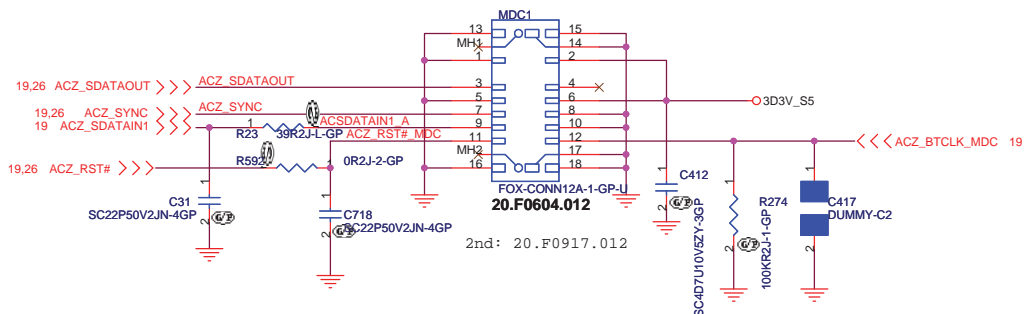


# ETOOTH MODULE

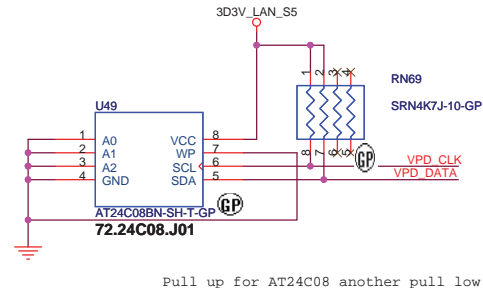
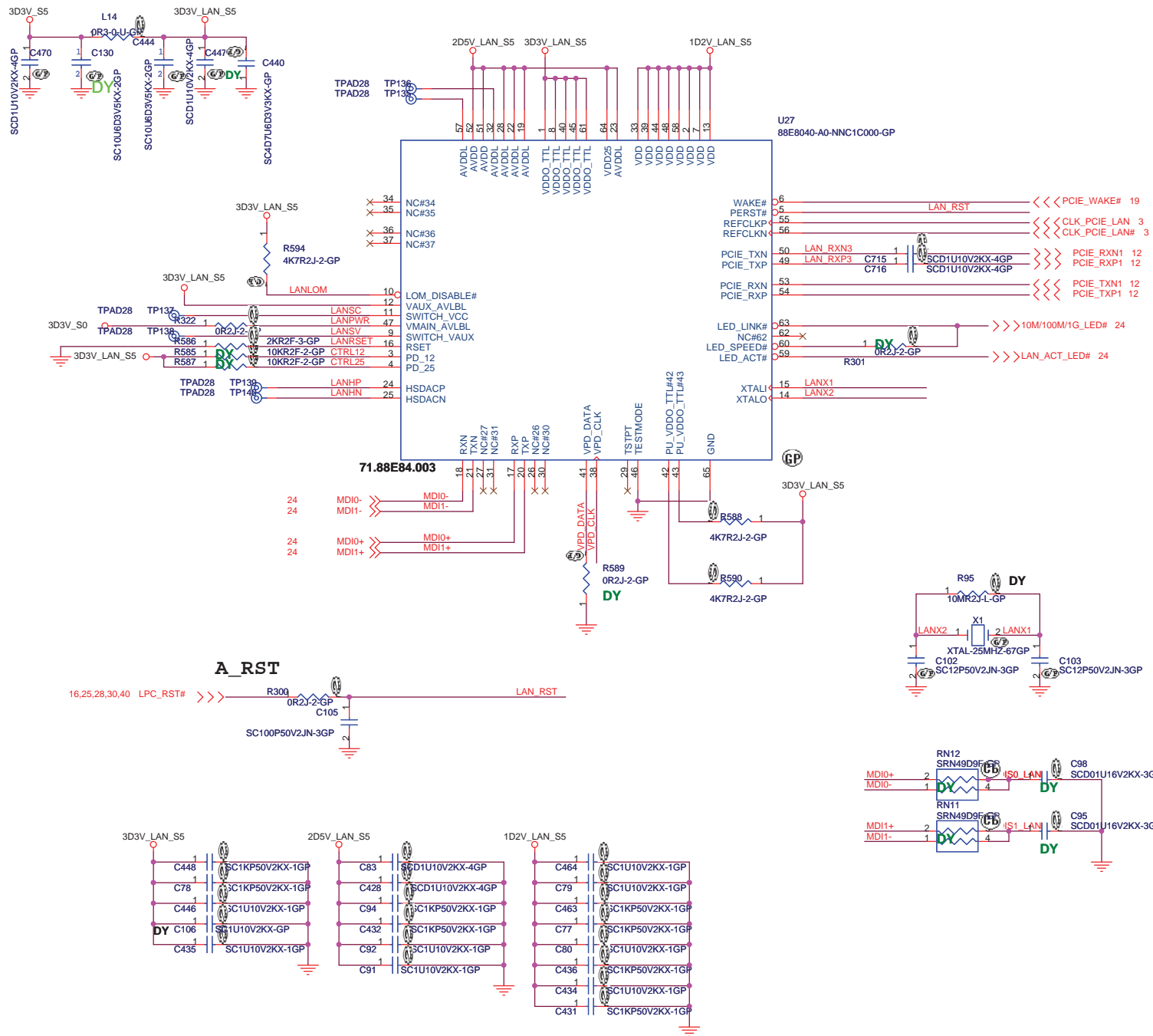
EC21 put near BLUE1 / all  
USB put one choke near connector by EMI request

20.D0197.104

The diagram shows four USB power lines (USBPN0, USBPP0, USBPN2, USBPP2) connected to four EC modules (EC168, EC169, EC170, EC171). Each module has a green 'DY' label and a '2' in a circle, indicating a 2A current rating. The modules are connected to a common ground. The USBPP0 line is connected to the positive terminal of each module's power input. The USBPN2 line is connected to the negative terminal of each module's power input. The USBPN0 and USBPP2 lines are connected to the positive terminal of each module's power input. The USBPP0 line is connected to the negative terminal of each module's power input.

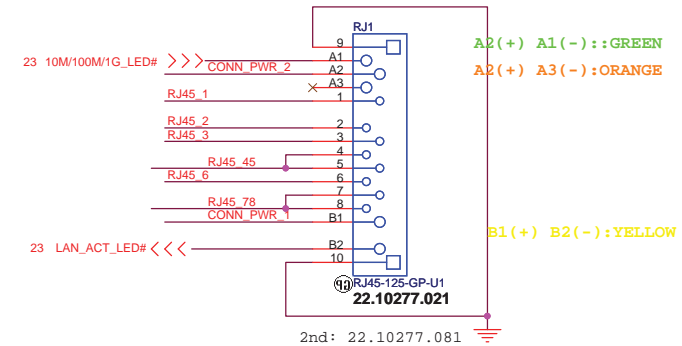
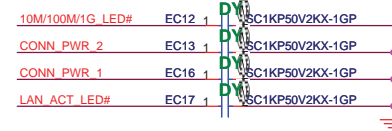




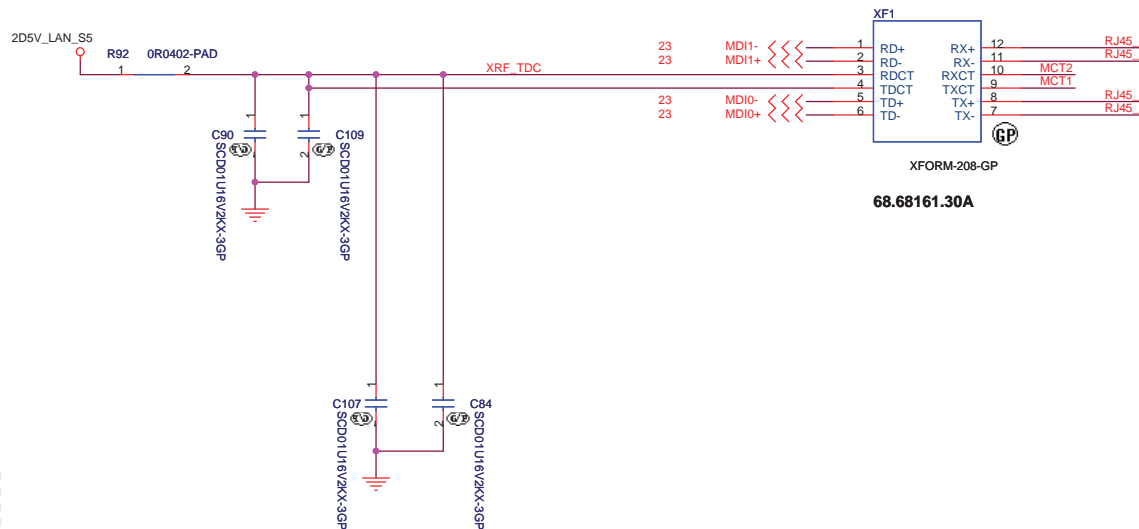


Pull up for AT24C08 another pull low

# LAN Connector



## 10/100 Lan Transformer

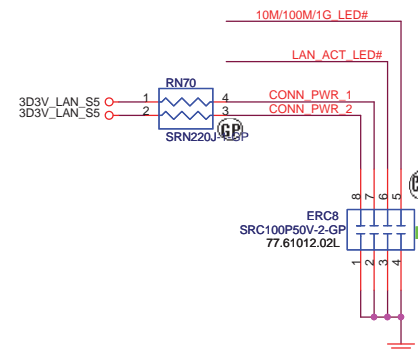
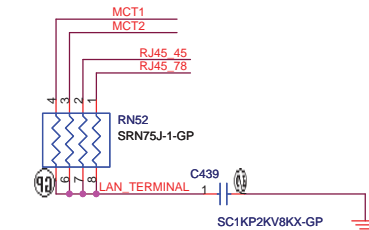


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

**RJ11 signal must leave the other signal or power plane 100mil.**

DOC\_TIP,DOC\_RING,TIP,RING:  
 W/S : 10/100 @ Surface layers  
 10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

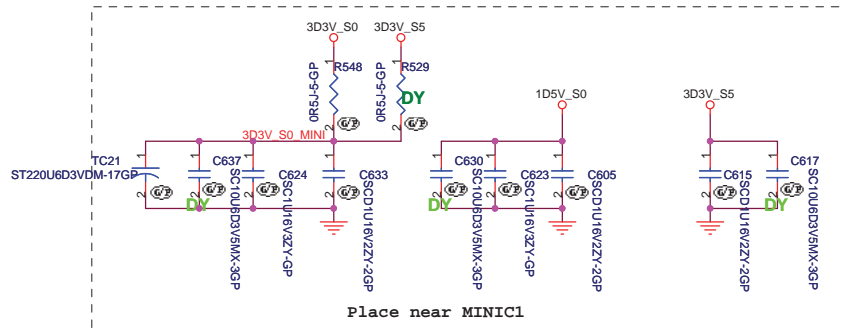
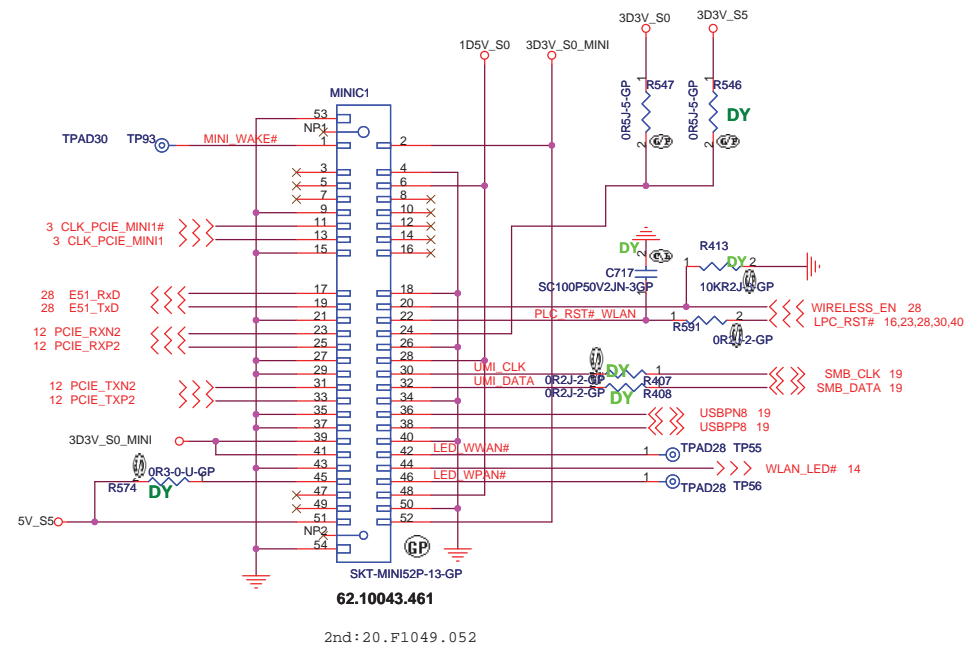
Title: **LAN Connector**

Size A3 Document Number: **Yukon** Rev: **SA**

Date: Thursday, July 03, 2008 Sheet 24 of 43

NEWCARD Connector

Mini Card Connector

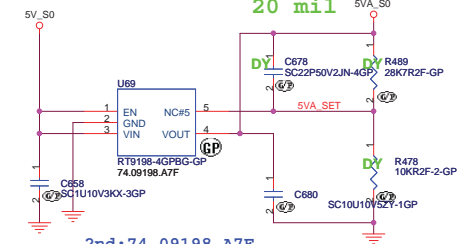


bom1

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MINI CARD / NEW CARD	
Size	Document Number
Yukon	
Date: Thursday, July 03, 2008	Sheet 25 of 43
Rev	SA

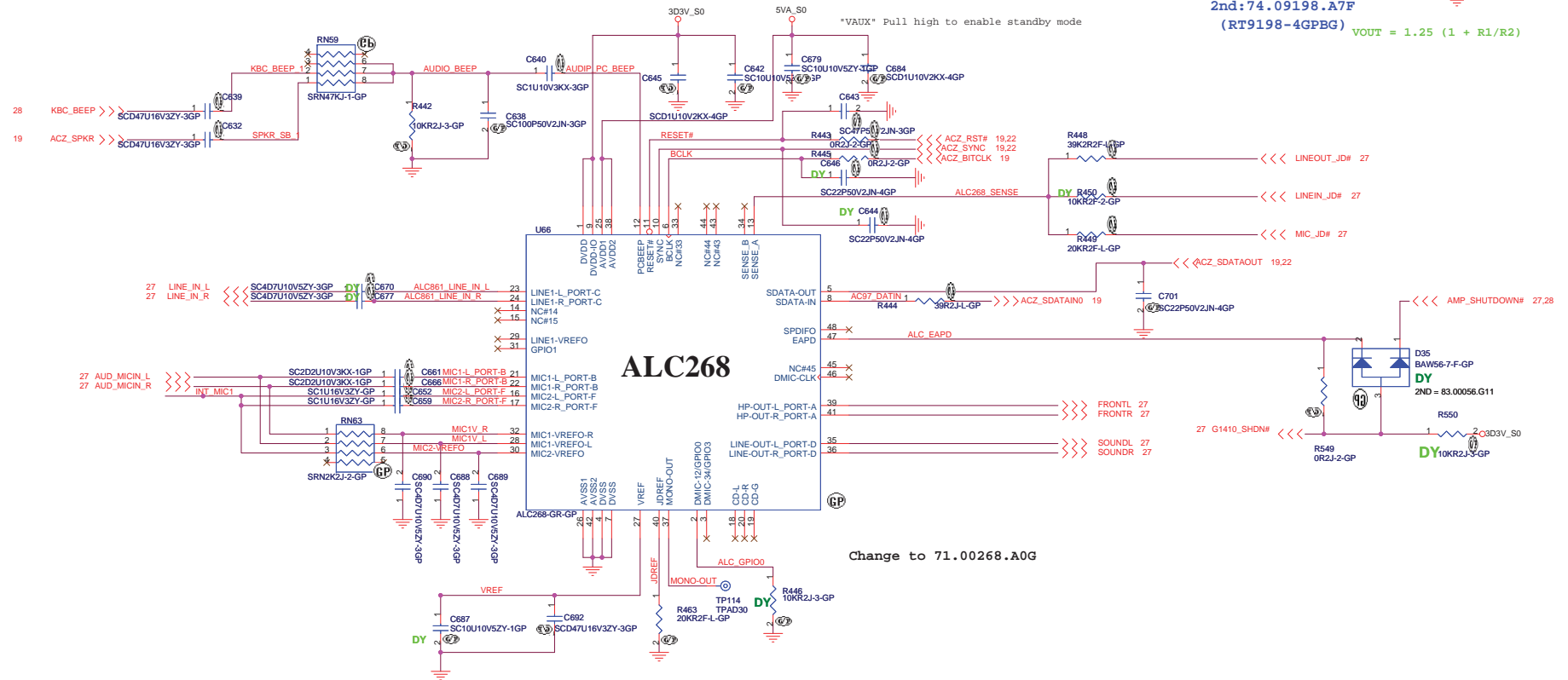
## POWER GENERATE

\*Layout\*  
20 mil 5VA



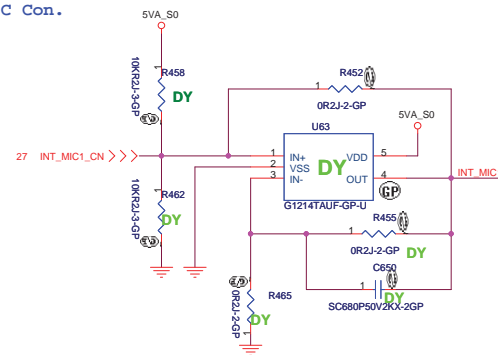
2nd:74.09198.A7F

(RT9198-4GPBG)

$$= 1.25 (1 + R1/R2)$$


Change to 71.00268.A0G

Near INTMIC Con.



<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>AZALIA CODEC - ALC268</b>
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Size	Document Number	Yukon
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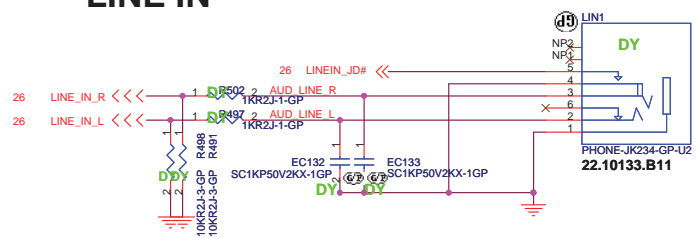
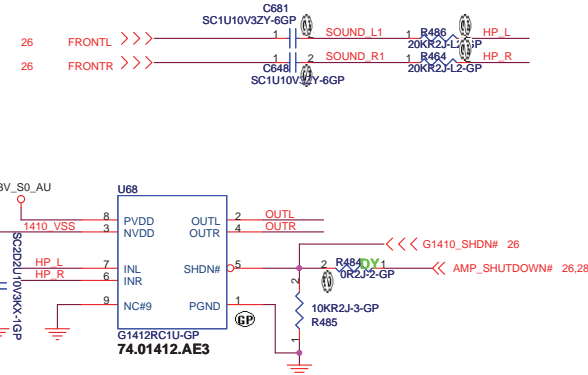
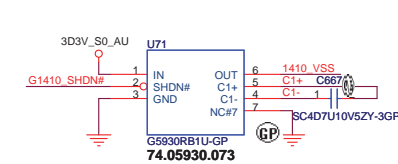
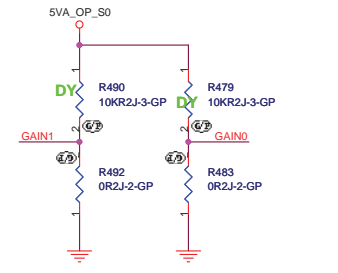
## Yukon

Rev	SA
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Date: Thursday, July 03, 2008

Sheet 26

	3
43	



26 INT\_MIC1\_CN >>>

EC31

10k

GP2

INTMIC1

ACES-CON2-1-GP2

20.D0197.102

2nd: 20.D0197.102

SPKR L-  
SPKR L+  
SPKR R-  
SPKR R+

EC162 EC163 EC164 EC165

SKRP50V20X-1GP SKRP50V20X-1GP SKRP50V20X-1GP SKRP50V20X-1GP

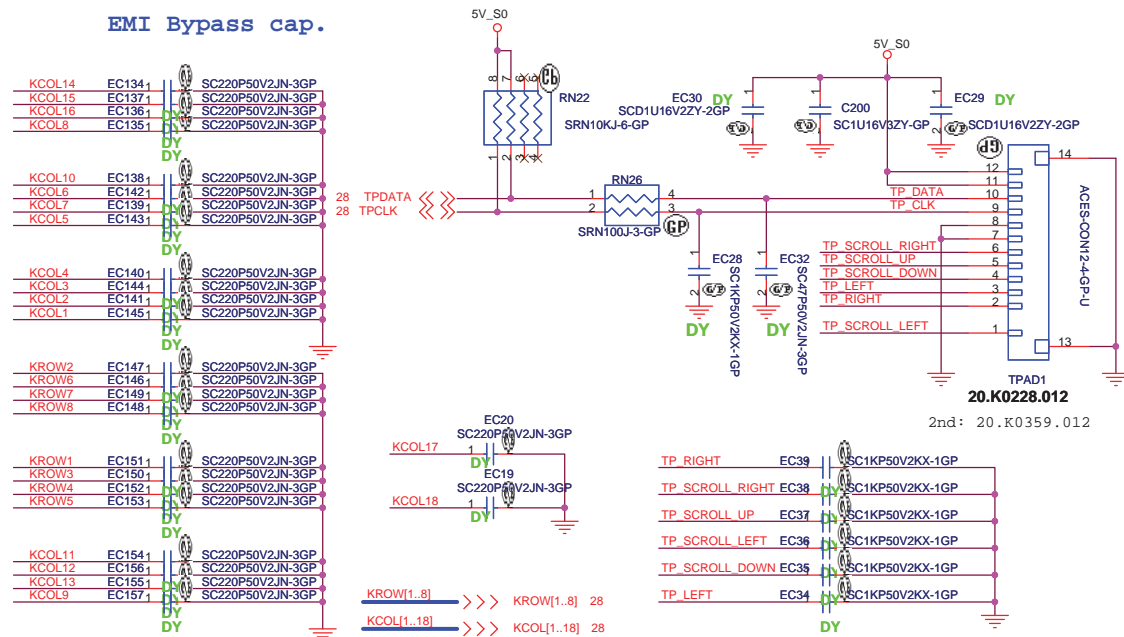
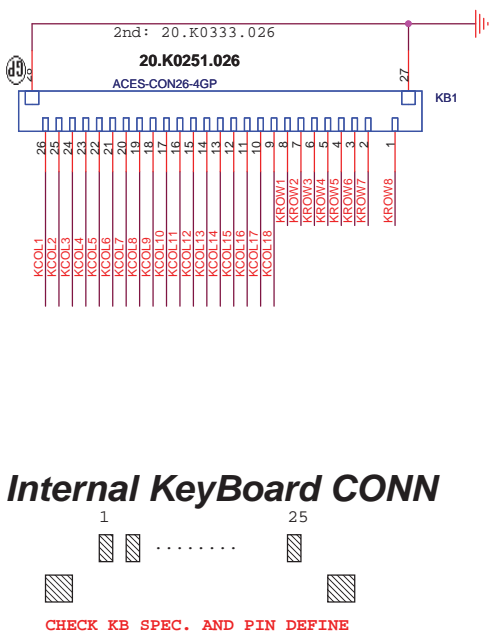
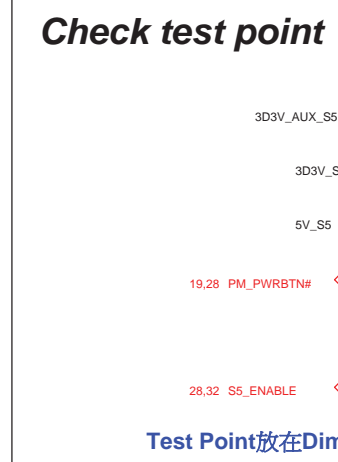
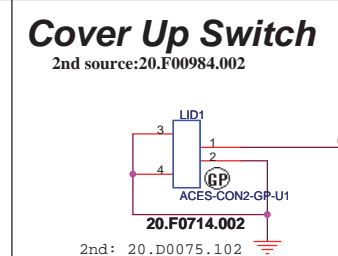
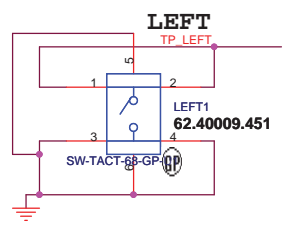
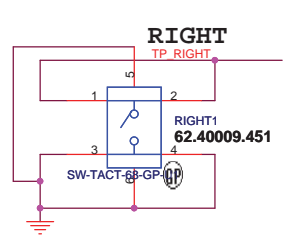
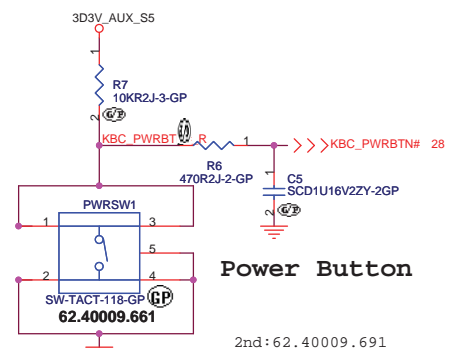
20.F0984.004

use Varistor for ESD solution

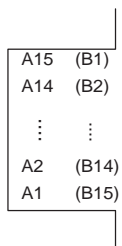
The schematic shows the MIC IN section. It includes two input signals, AUD\_MICIN\_R and AUD\_MICIN\_L, which are connected through resistors R493 and R495 respectively to pins 1 and 2 of a 1K2J1-3-GP component. A third signal, DTY, is connected through resistor R486 to pin 1 of a 0K6ZJ-3-GP component. The output of the 1K2J1-3-GP component is connected to pin 1 of a 1K2J1-1-GP component, which is also labeled MIC\_ID#. The output of the 0K6ZJ-3-GP component is connected to pin 2 of the same 1K2J1-1-GP component. The 1K2J1-1-GP component is connected to a microphone module (PHONE\_JK233-GP-US) via pins 1, 2, and 3. The microphone module is also connected to a ground symbol.

2nd: 22.10251.511





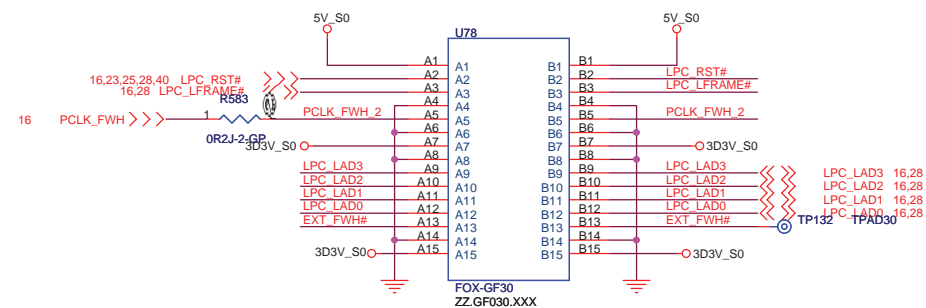
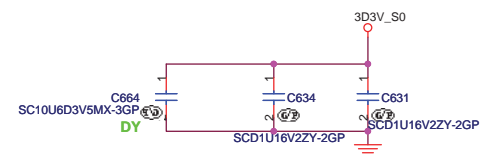


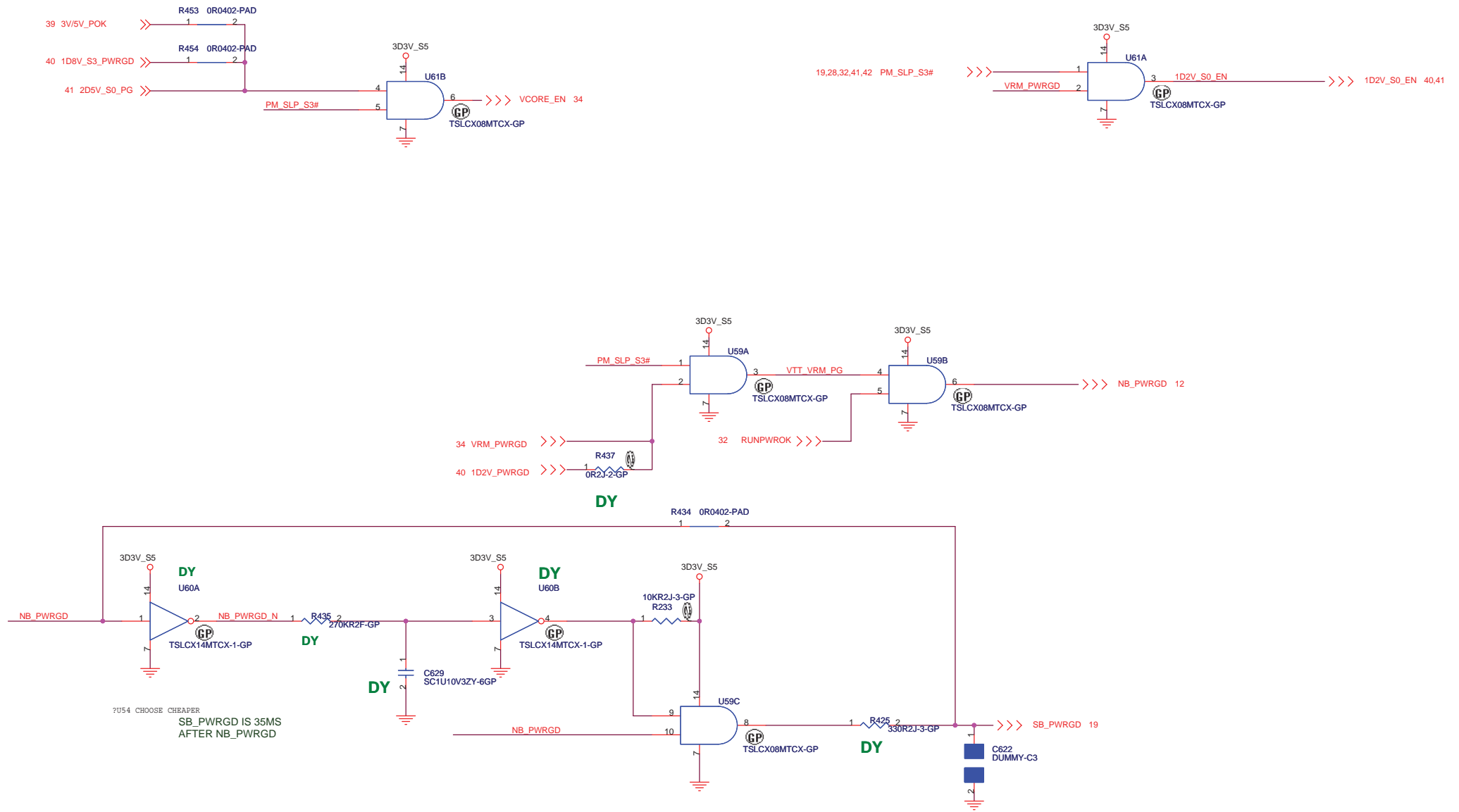


```

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

```

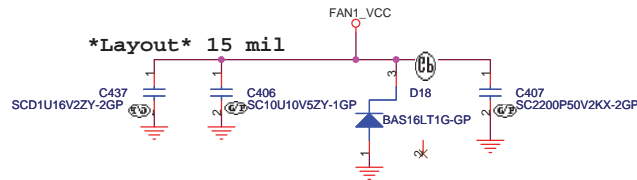




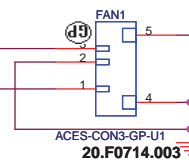
Setting T8 as 90 Degree

$$V\_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

\*Layout\* 15 mil

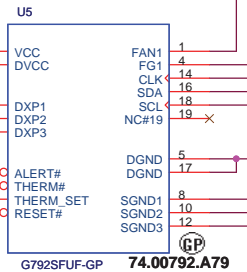
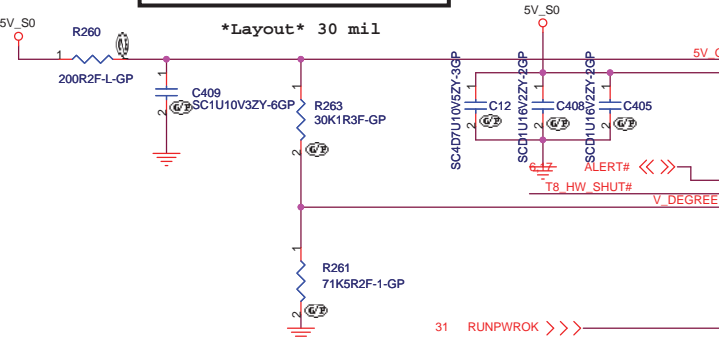


\*Layout\* 15 mil



2nd: 20.D0246.103

\*Layout\* 30 mil



DXP1:108 Degree  
DXP2:H/W Setting  
DXP3:88 Degree

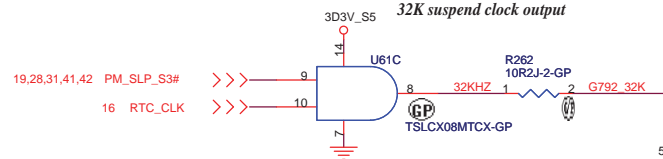
Place near chip as close as possible

2.System Sensor,  
Put between CPU and NB.

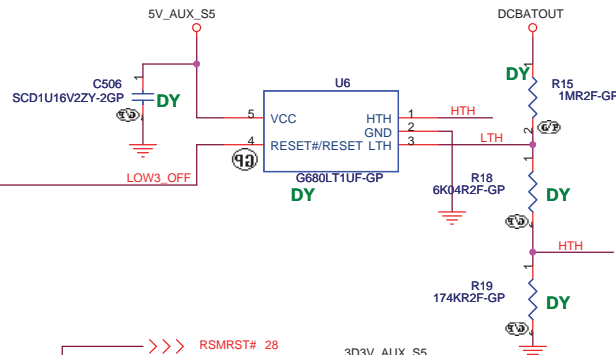
3.T8 Sensor

1.For CPU Sensor

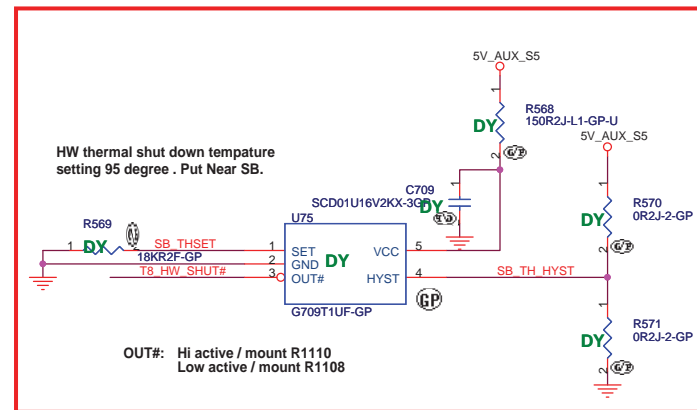
32K suspend clock output



HW Thermal Throttling BL3#



HW thermal shut down temperature  
setting 95 degree . Put Near SB.



OUT#: Hi active / mount R1110  
Low active / mount R1108

28,29 S5\_ENABLE >>>

S5PWR\_ENABLE 39

<<< KBC\_THERMTRIP# 6,28

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

G792

Size

A3

Document Number

Yukon

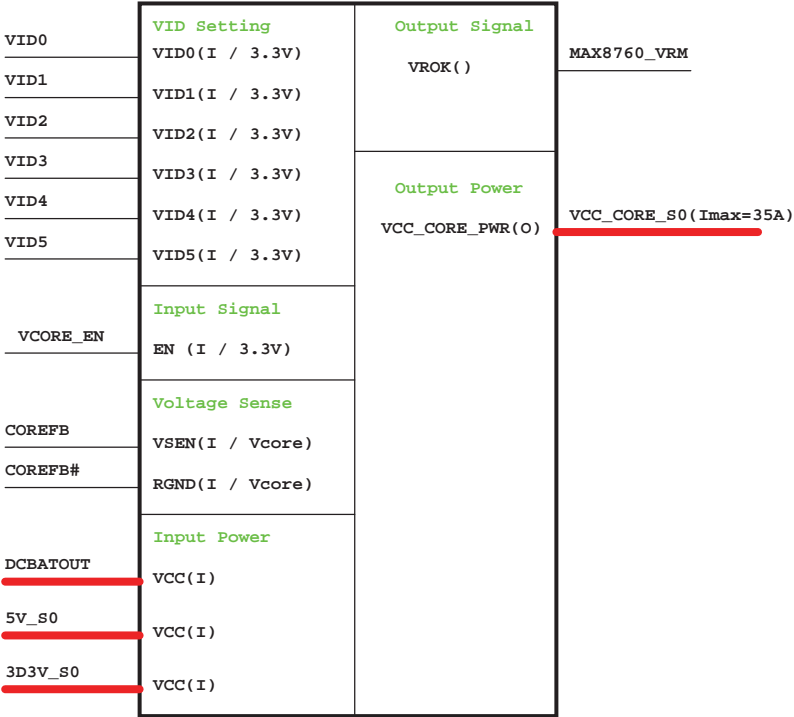
Rev

SA

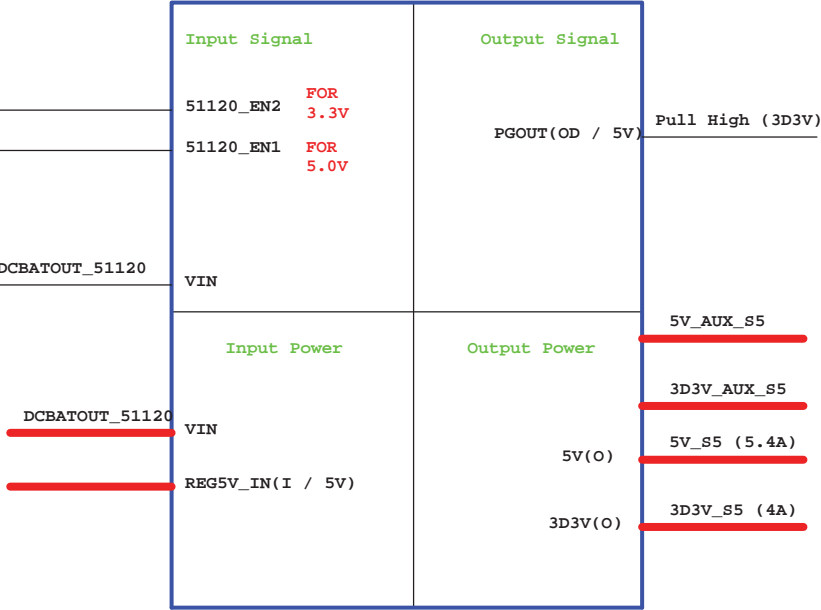
Date: Thursday, July 03, 2008

Sheet 32 of 43

CPU\_CORE  
ISL6264CRZ



TI TPS51120  
3D3V/5V



2D5V\_S0



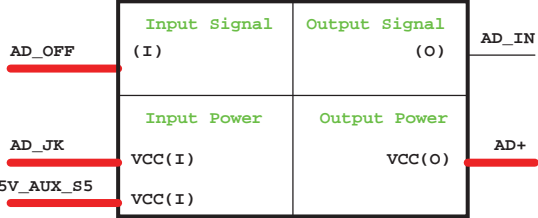
APL5913

1D8V\_S5

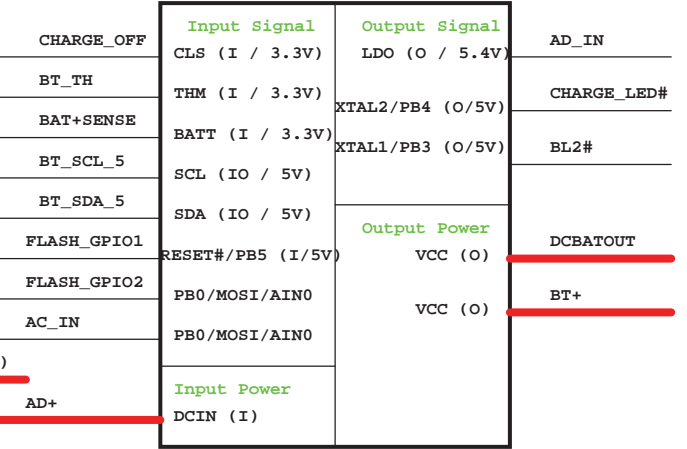


APL5332KAC-TRLGP

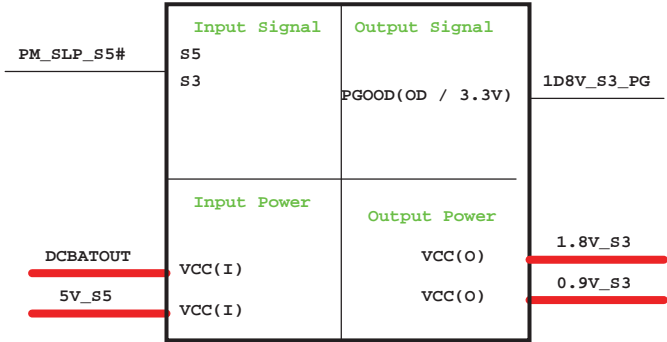
Adapter



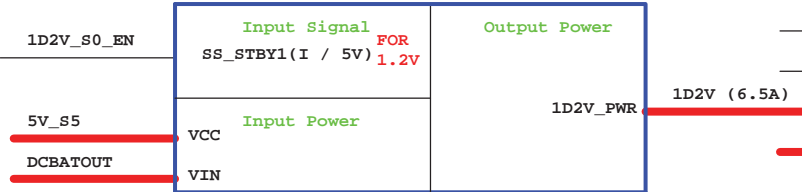
Charger\_ISL6255



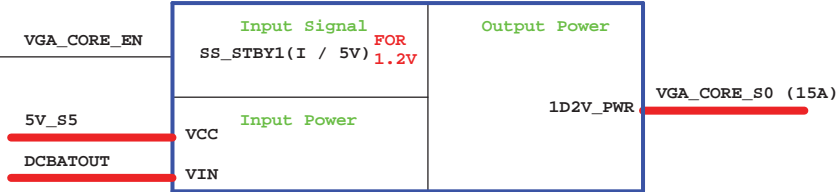
TI TPS51116  
1.8V / 0.9V



ISL6268\_1D2V



ISL6268\_VGA\_CORE

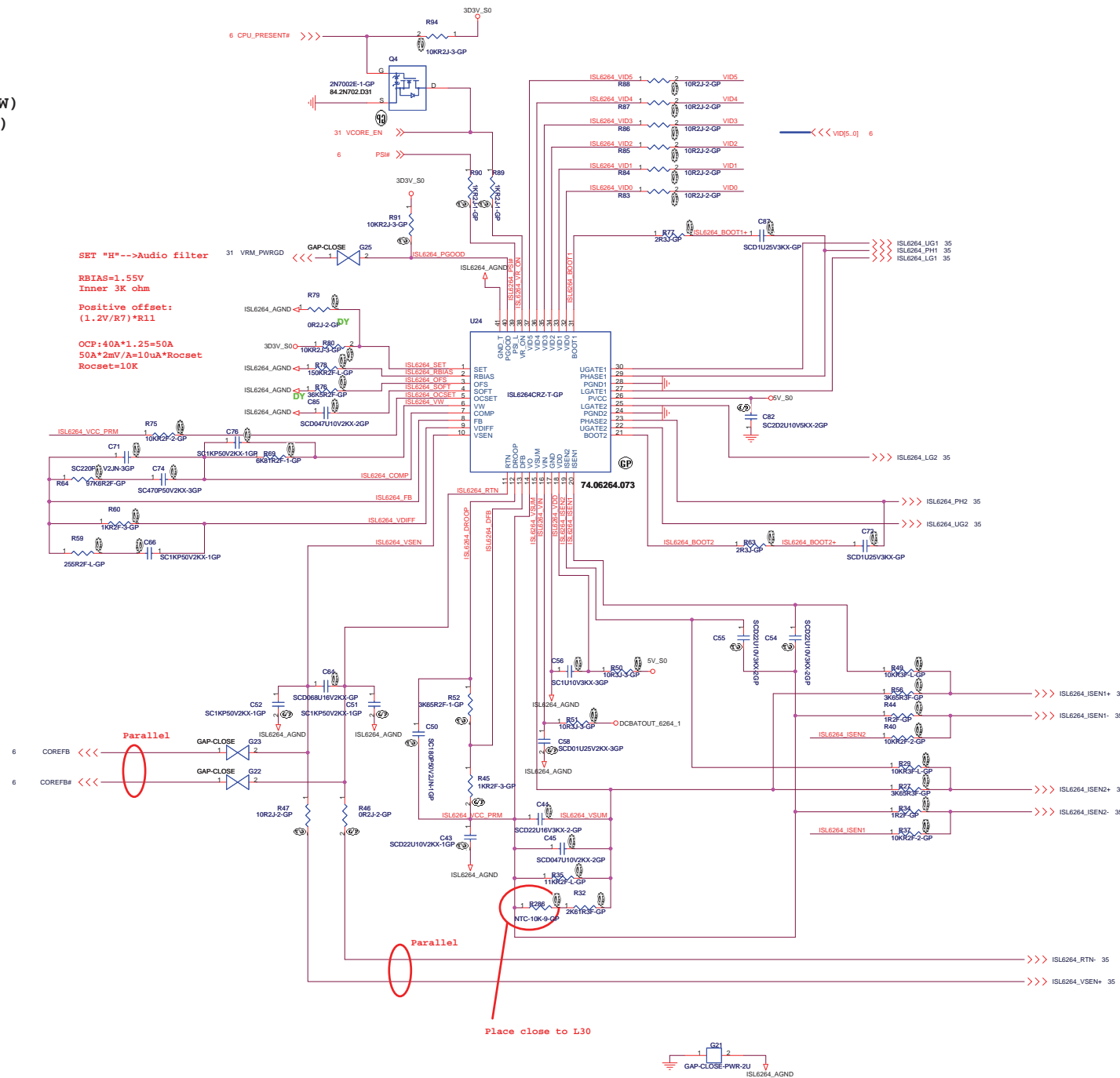


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<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>Power Block Diagram</b>		
Size A3	Document Number <b>Yukon</b>	Rev <b>SA</b>
Date: Tuesday, July 01, 2008	Sheet 33 of 43	

VID=1.20V(25W)/1.15V(35W)  
Iomax=21A(25W)/35A (35W)  
OCP=40A~45A

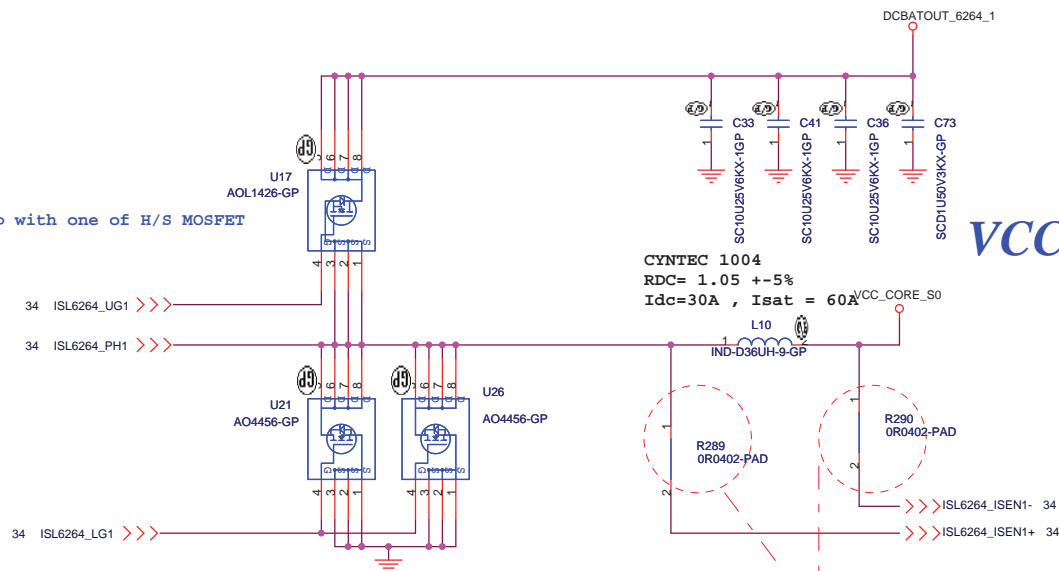
V1D5	V4D4	V3D3	V2D2	V1D1	V0D0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	1	0	1.525
0	0	0	0	1	1	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	0	1	1	1	1.375
0	0	1	0	0	0	1.350
0	0	1	0	0	1	1.325
0	0	1	0	1	0	1.300
0	0	1	0	1	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	0	1	1.225
0	0	1	1	1	0	1.200
0	1	0	0	0	0	1.175
0	1	0	0	0	1	1.150
0	1	0	0	1	0	1.125
0	1	0	0	1	1	1.100
0	1	0	1	0	0	1.075
0	1	0	1	0	1	1.050
0	1	0	1	1	0	1.025
0	1	0	1	1	1	1.000
0	1	1	0	0	0	0.975
0	1	1	0	0	1	0.950
0	1	1	0	1	0	0.925
0	1	1	0	1	1	0.900
0	1	1	1	0	0	0.875
0	1	1	1	0	1	0.850
0	1	1	1	1	0	0.825
0	1	1	1	1	1	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7125
1	0	0	1	0	0	0.7
1	1	1	1	1	1	0.375



Place close to L30

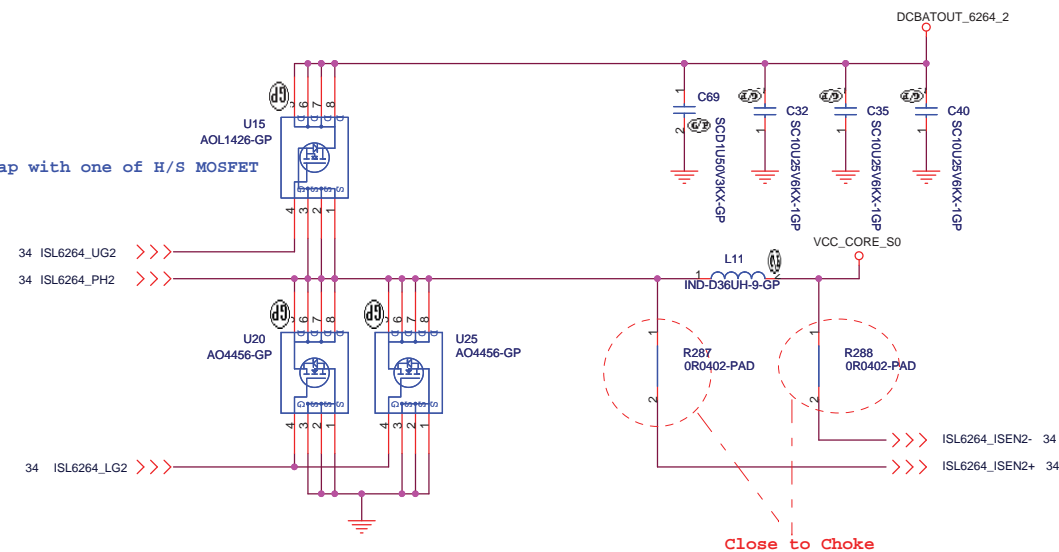


Overlap with one of H/S MOSFET

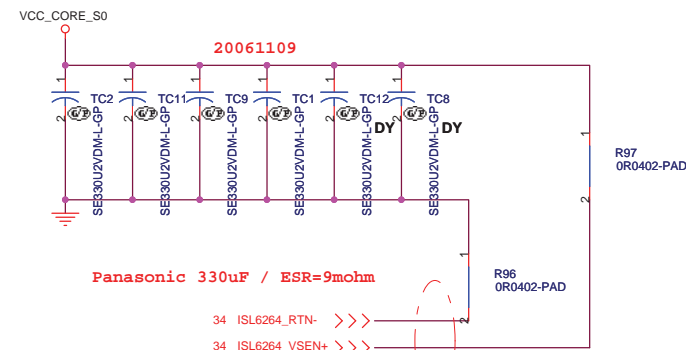
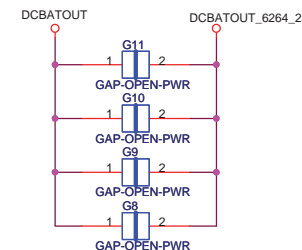
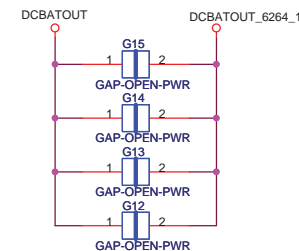


Close to Choke

Overlap with one of H/S MOSFET



Close to Choke

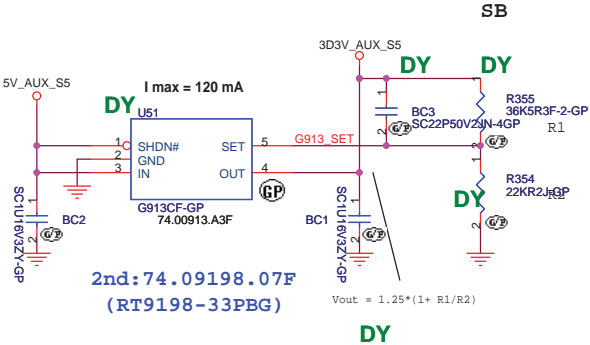


<Core Design>

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
CPU Vcore Power_2		
Size A3	Document Number	Rev SA
Yukon		
Date: Thursday, July 03, 2008	Sheet 35 of 43	

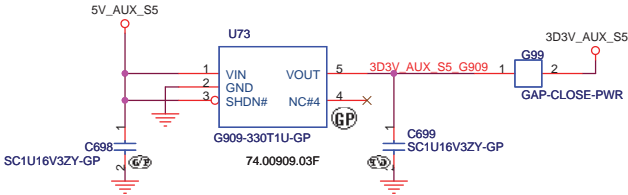
Aux Power

3D3V\_AUX\_S5

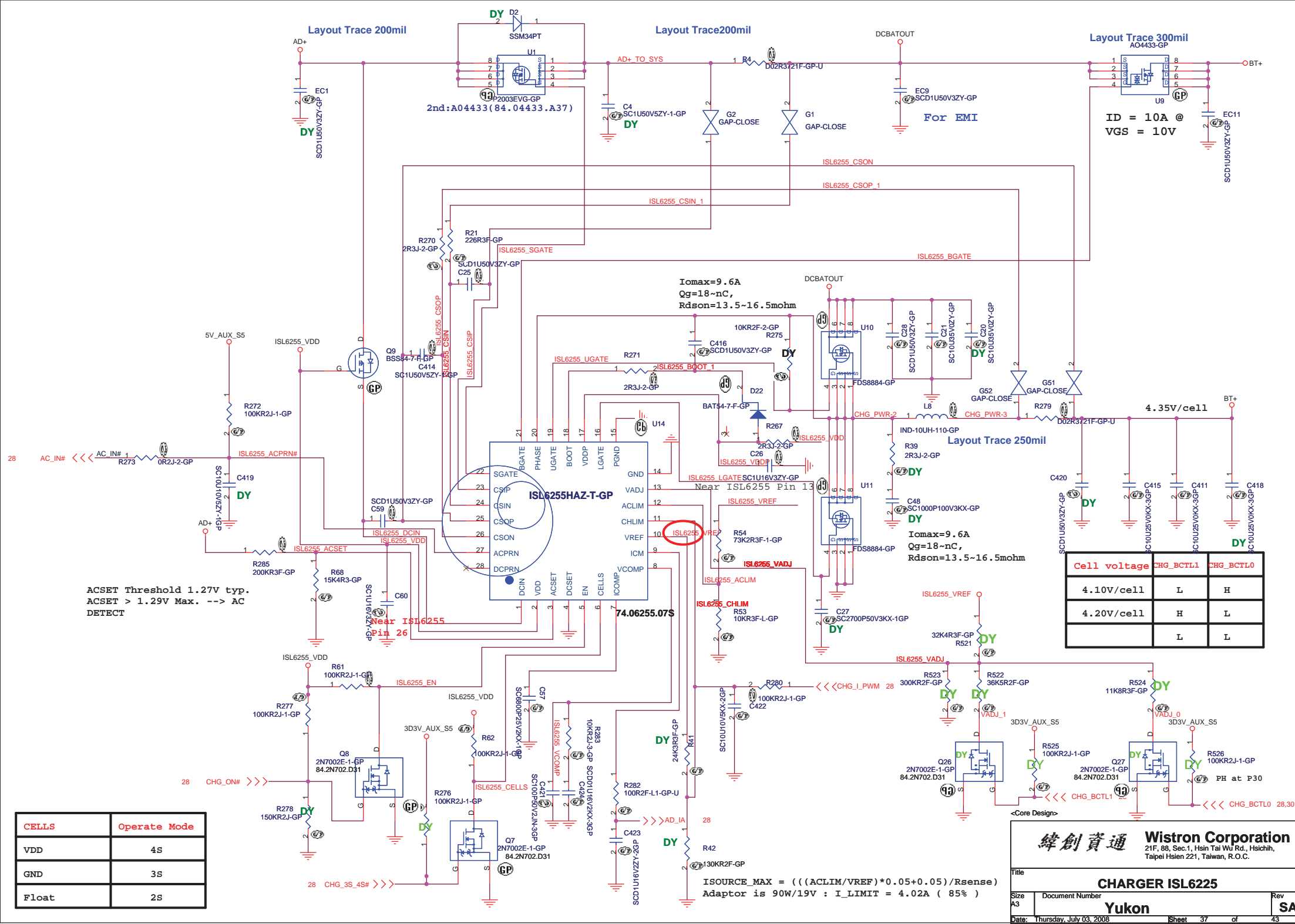


Aux Power

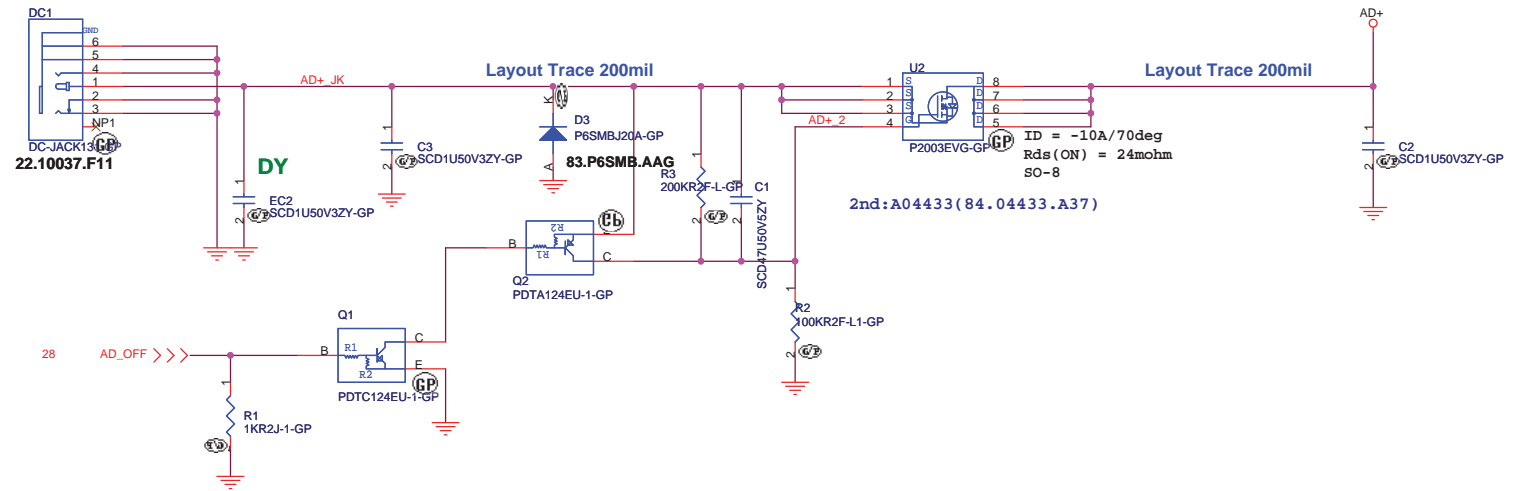
3D3V\_AUX\_S5



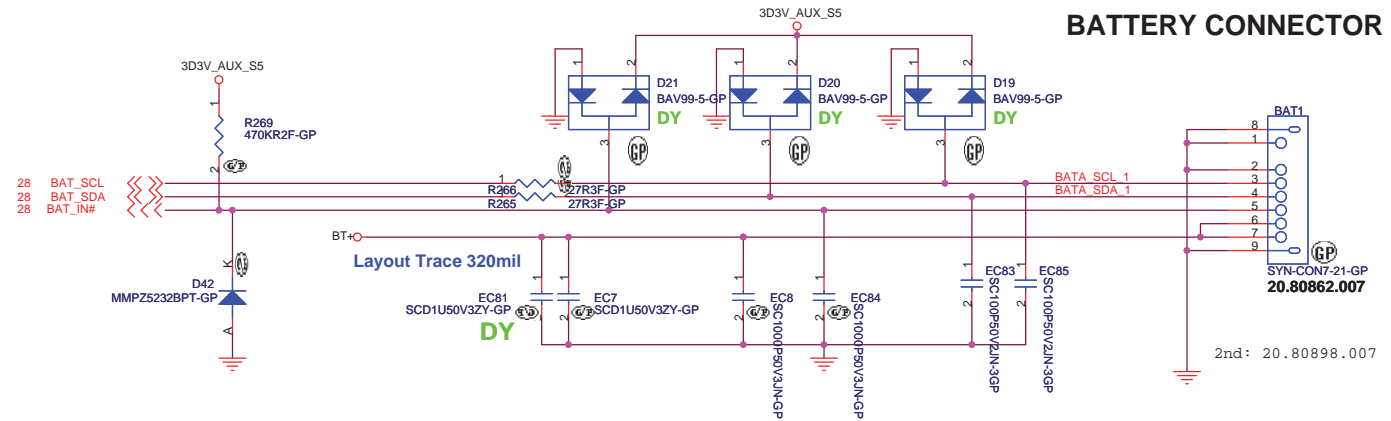




# Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



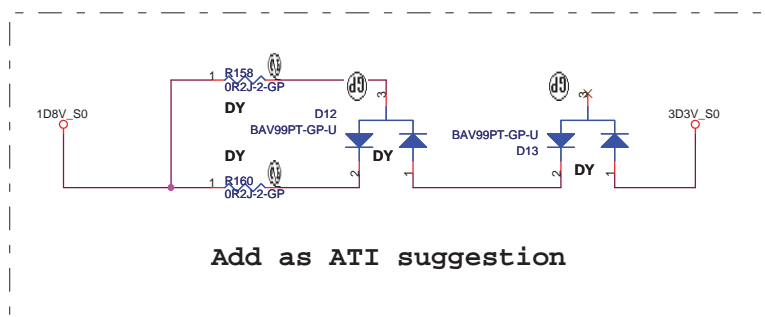
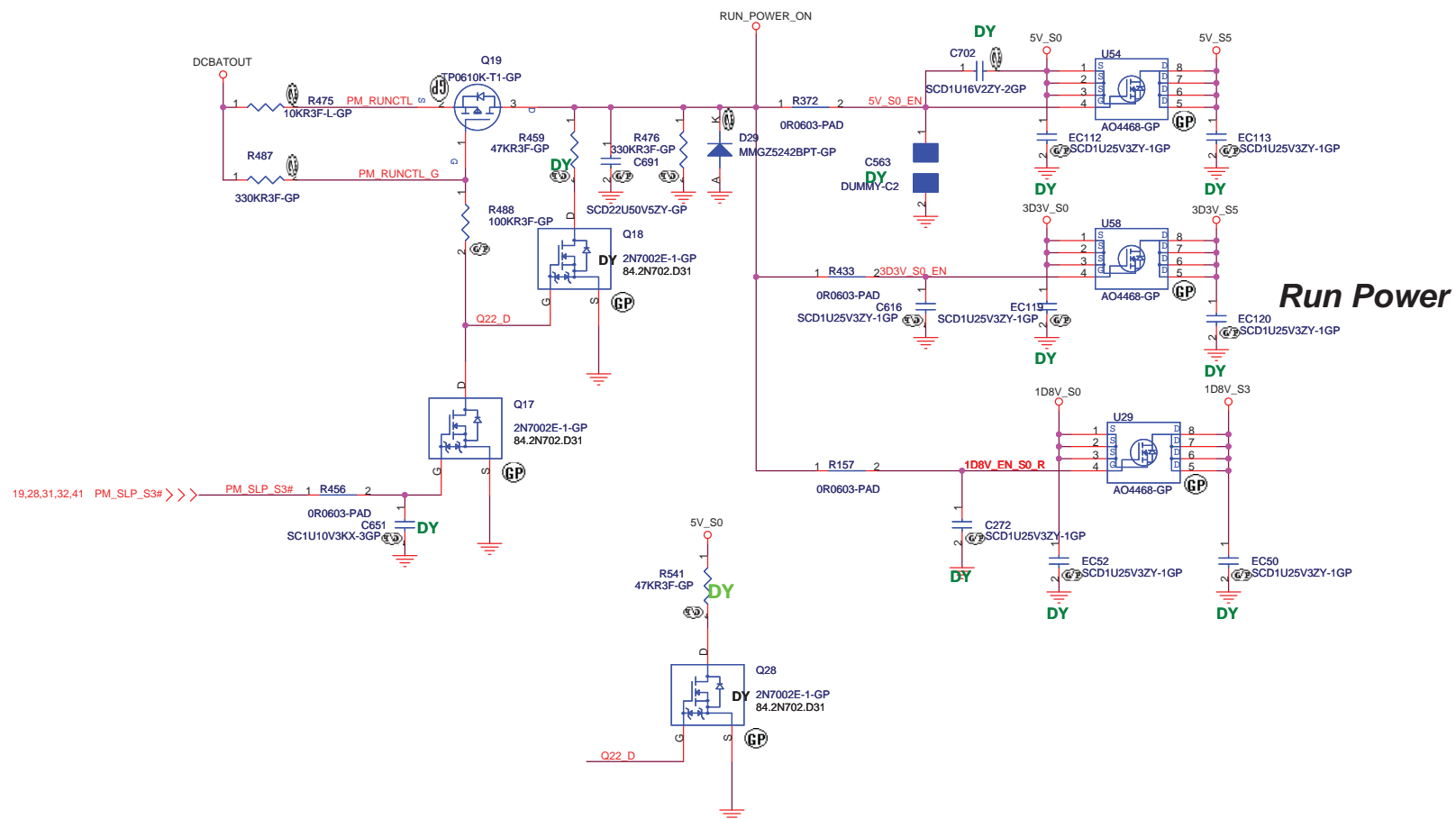
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<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>AD/BATT CONN</b>	
Size A3	Document Number <b>Yukon</b>
Date: Thursday, July 03, 2008	Rev <b>SA</b>
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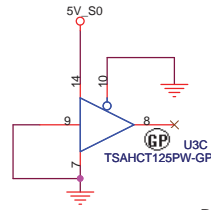
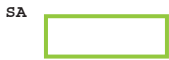




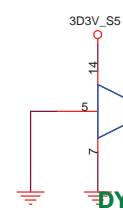
## Power On Logic

<Core Design>

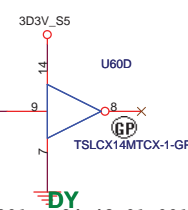
<b>緯創資通</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>RUB POWER</b>			
Size A3	Document Number <b>Yukon</b>	Rev SA	
Date: Thursday, July 03, 2008		Sheet 42 of 43	



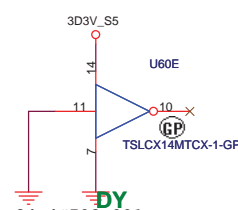
DUMMY in SA



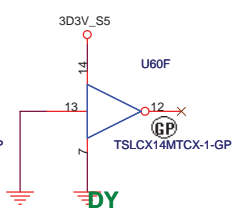
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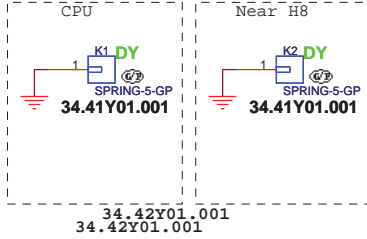
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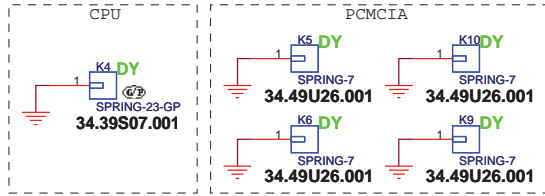
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34.42Y01.001



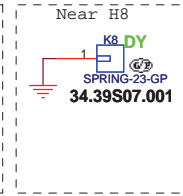
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34.42Y01.001



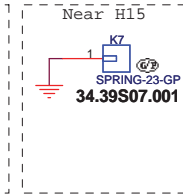
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34.49U26.001

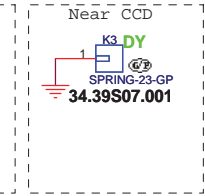
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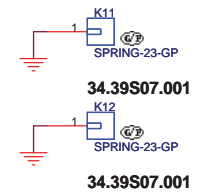
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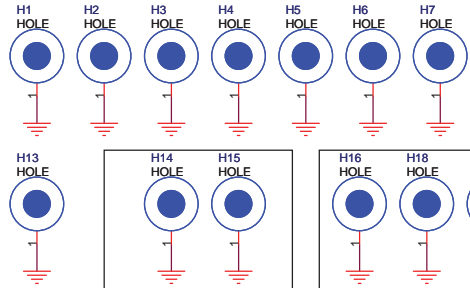


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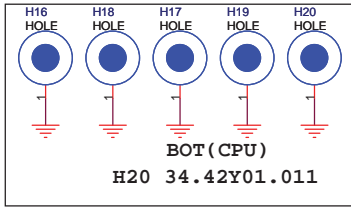


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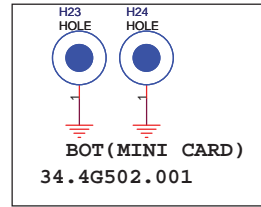
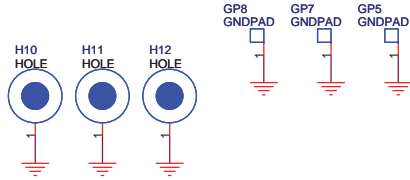
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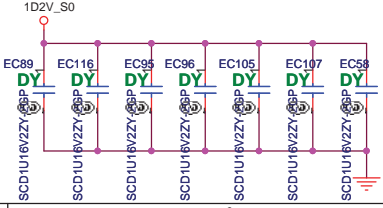
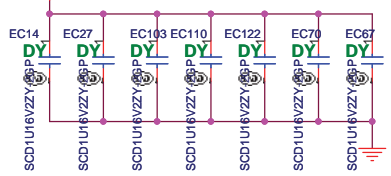
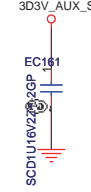
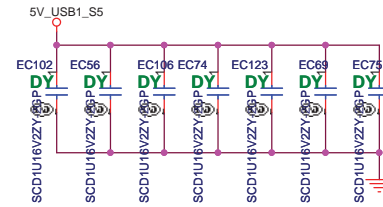
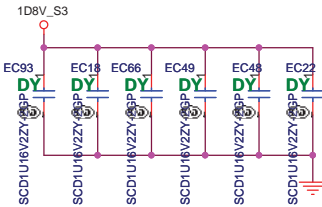
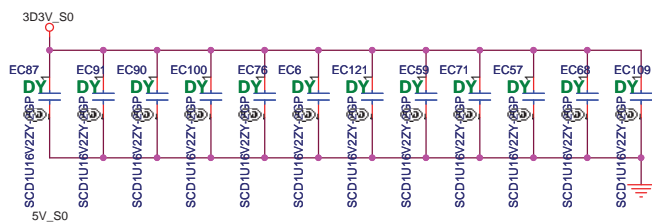
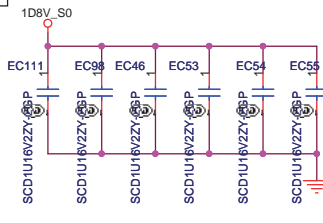
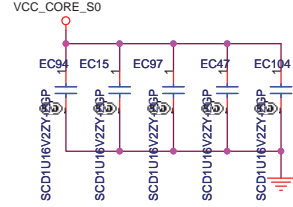
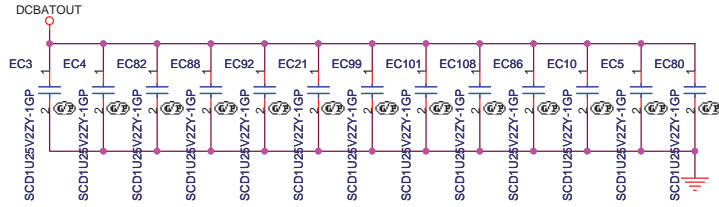
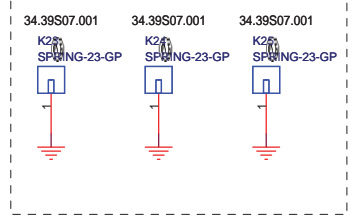
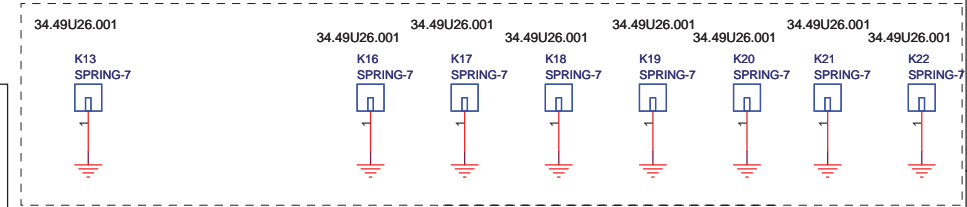
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34.42Y01.011



BOT (CPU)  
H20 34.42Y01.011



BOT (MINI CARD)  
34.4G502.001



<Core Design>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		Rev
EMI/Spring/Boss		
Size	Document Number	SA
Date: Thursday, July 03, 2008		
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